

TITLE	Page
Cover Sheet	1
Block Diagram	2
CPU-Memory, CPU-PEG/Display	3,4
CPU-Control/MISC/CFG/Audio	5
CPU-Power,CPU-GND	6,7
DDRIII DIMM1&DDRIII DIMM1	8,9
PCH-USB/PCIE/DMI/SATA	10
PCH-Audio/Display/Clock	11
PCH-GPIO/USBOC#/SATASTRAP	12
PCH-LPC/SPI/SMBUS/MISC	13
PCH-Power,PCH-GND,PCH-Strap	14,15,16
PCIE SLOT-CPU(X16) PCIE SLOT-PCH(X1)	17,18
SIO-NCT6793D/PS2 / COM Port	19,20
ASM1083 PCI Bri. / PCI_X2 Slot	21,22
FAN CONTROLLOR / AUDIO - ALC892/887	23,24,25
LAN - RTL8111H	26
DVI/VGA	27,28
USB2.0/USB3.0/SATA connector	29,30,31
CUT_VBAT circuit/BIOS ROM	32,33
ACPI CONTROLLER	34
PWM-RT3606BC/VCORE 3PHASE/VGT 2PHASE	35,36,37
DDR-RT8231AGQW	38
PCH Core power / CPU PWR_ST/PLL	40
VCCSA - POWER	41
VCCIO - POWER / CPU PWR_ST/PLL	42
ATX F_Panel/TPM/MSI_LED	43
DEBUG LED/EMI CAP/Manial Part	44,45,46
Power Map/GPIO MAP/Power Sequence	47,48,49
Revision History	50

MS-7A49

ATX:205*243

Ver: 1.0

Intel -SkyLake-S plamform

CPU:

LGA1151
CPU POWER PAK *3 Phase(1/2)
GT POWER PAK *2 Phase(1/1)

System Chipset:

PCH-H :H110

Onboard Chip:

HD Audio Codec: ALC887
SIO: NCT6793D
Flash ROM: SPI 64 Mb
DP to VGA: ITE6515

PWM:

VCORE - RT3606BC
DDR - RT8231AGQW
PCH(1.0V) - RT8125C
VCCSA - RT8125C
VCCIO - SLG59M1457V Load Switch

Main Memory:

DDR4 * 2 (Dual Channel)

LDO:

VCCSTPLL - GS7166

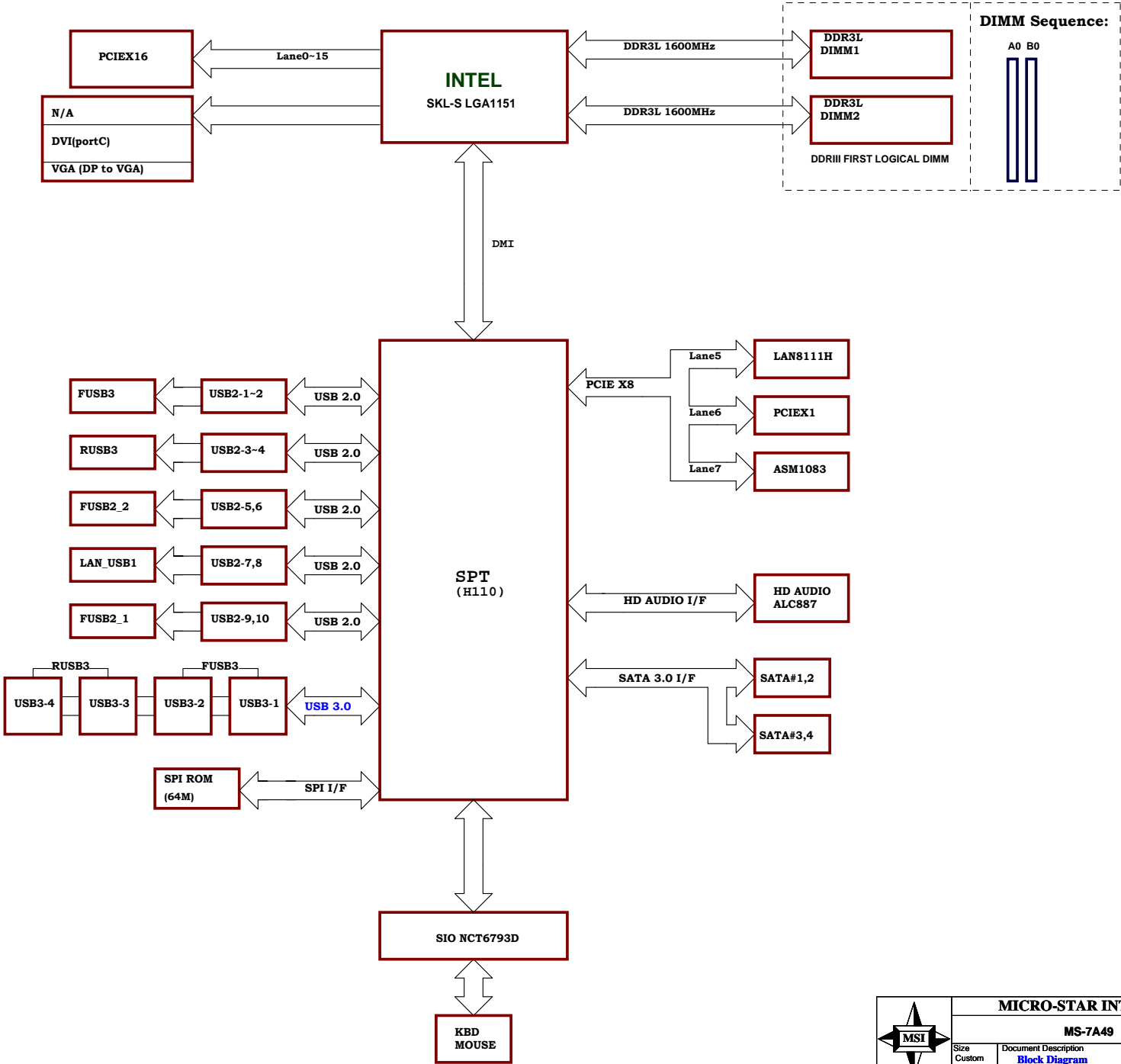
ACPI:

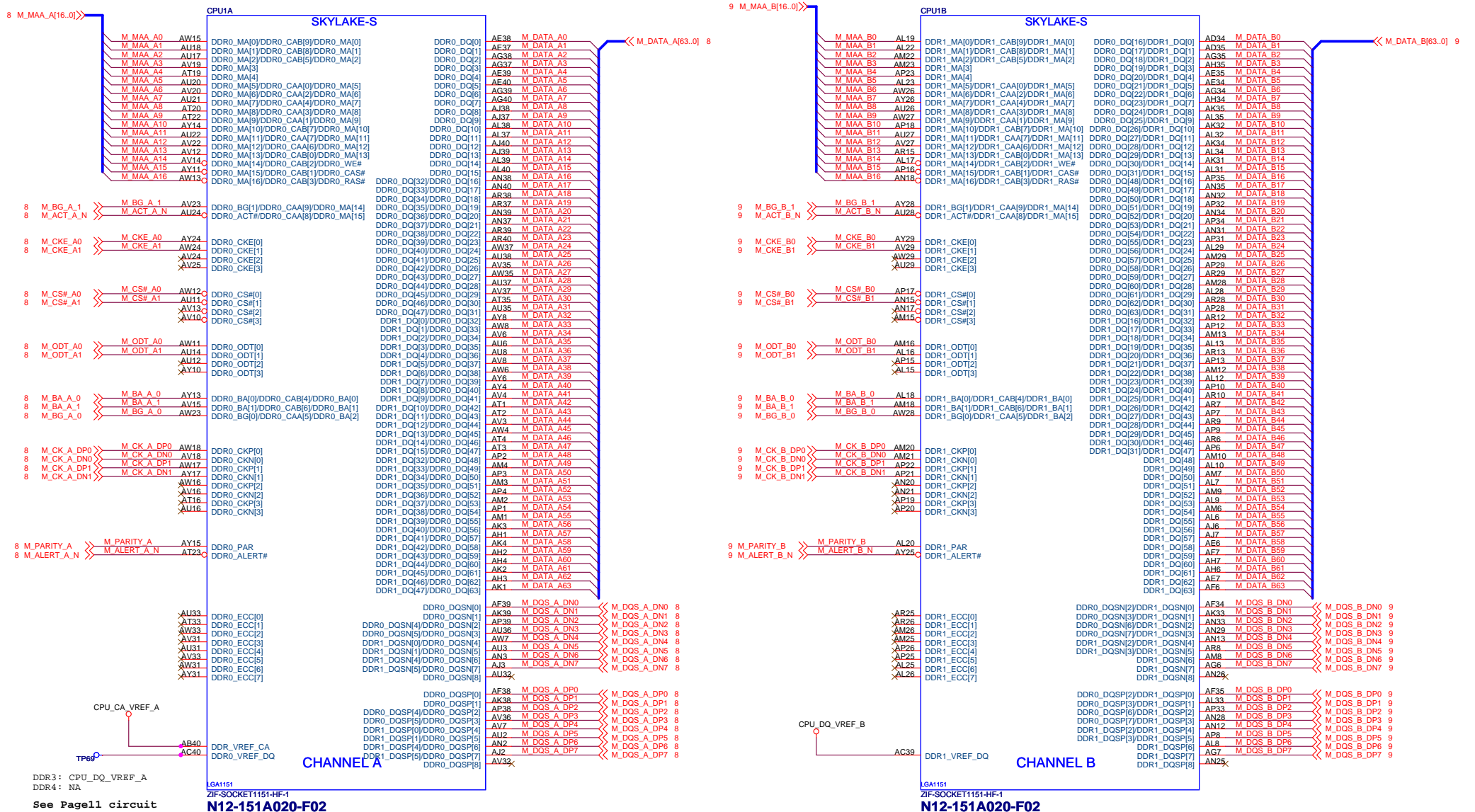
5VDAUL:uP7501
5VDIMM:uP7501
3VSB:GS7166+PN MOS
3VDSW:GS7166

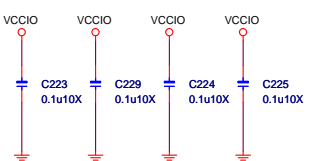
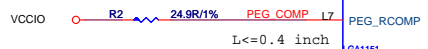
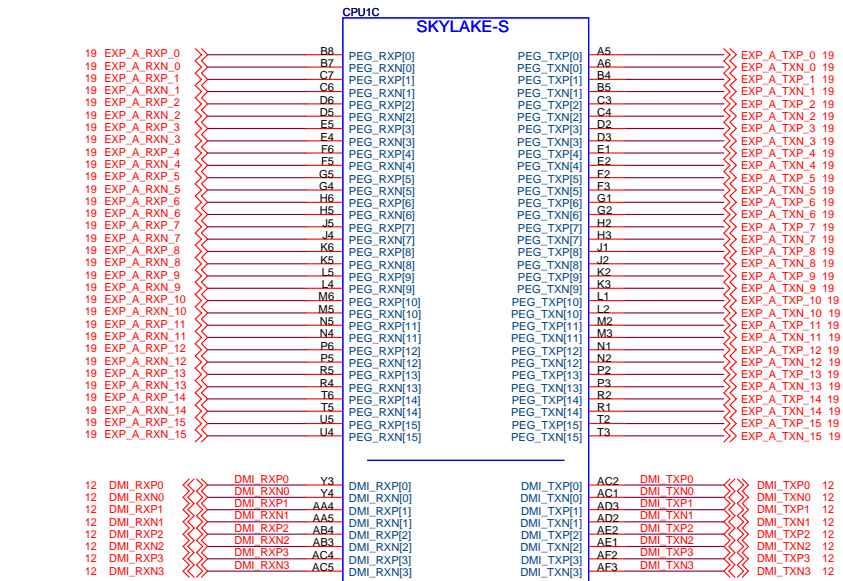
Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 1
PCI Slot * 2

MS-7981 Block Diagram

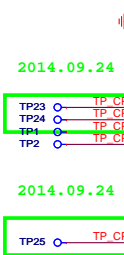




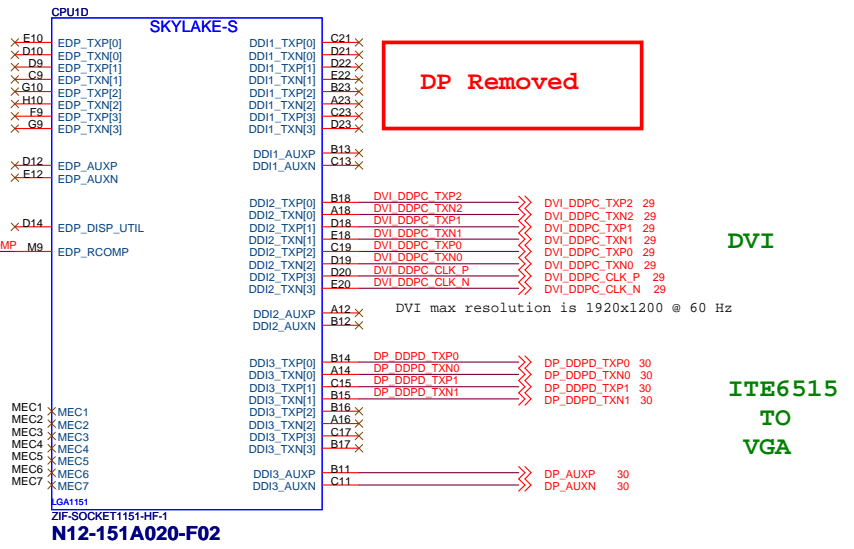
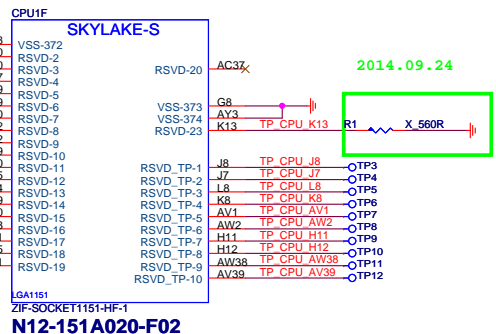


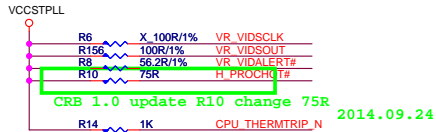
For DMI reference VCCIO USE
please close to DMI via side

CRB 1.0 update
Add TP23,TP24
For Test



CRB 1.0 update
TP25
For Test





2014.08.14

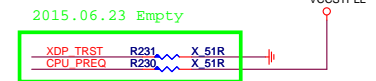
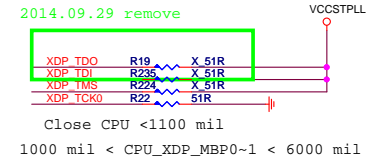
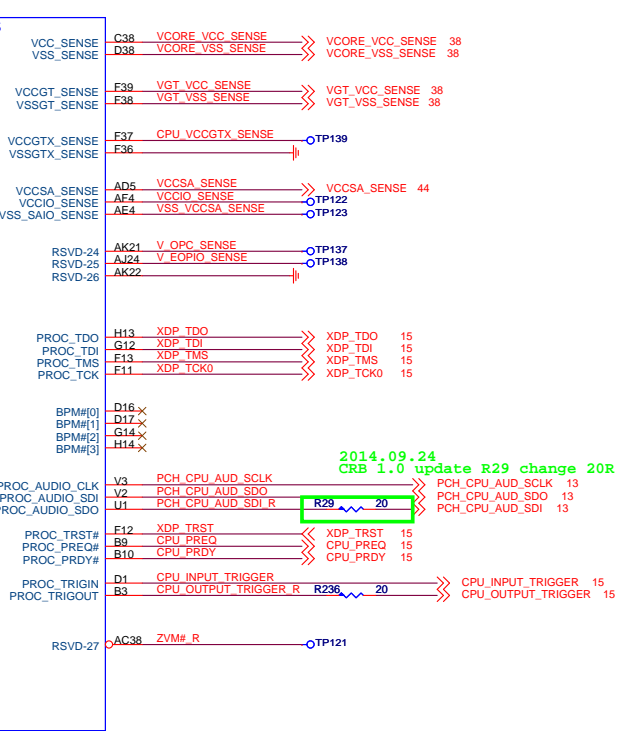
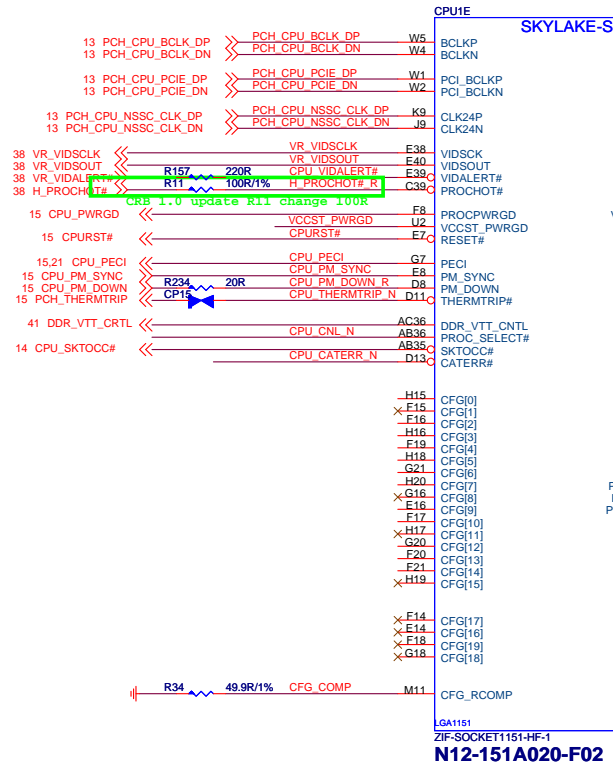
This pin is for compatibility with future platforms. It should be unconnected for SKL. for KDS0.85 page.117

R136 1K CPU_CN_L_N

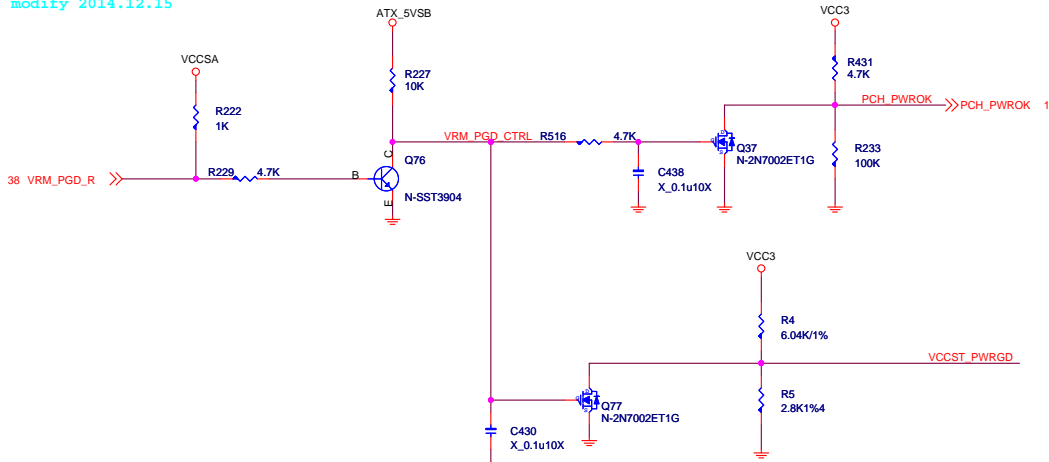
VCCSTPLL R228 10K CPU_CATERR_N

CFG Strap

CFG Table			
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CPGSEL(0)
6	DISABLE	ENABLE	PEG0CPGSEL(1)
7	RESET#	BIOS REQ	PEG_DEFR_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		RSVD
15	RSVD		RSVD

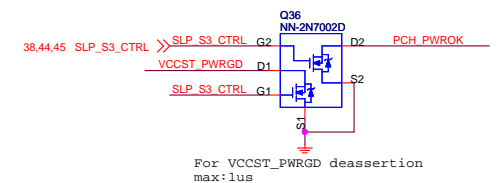


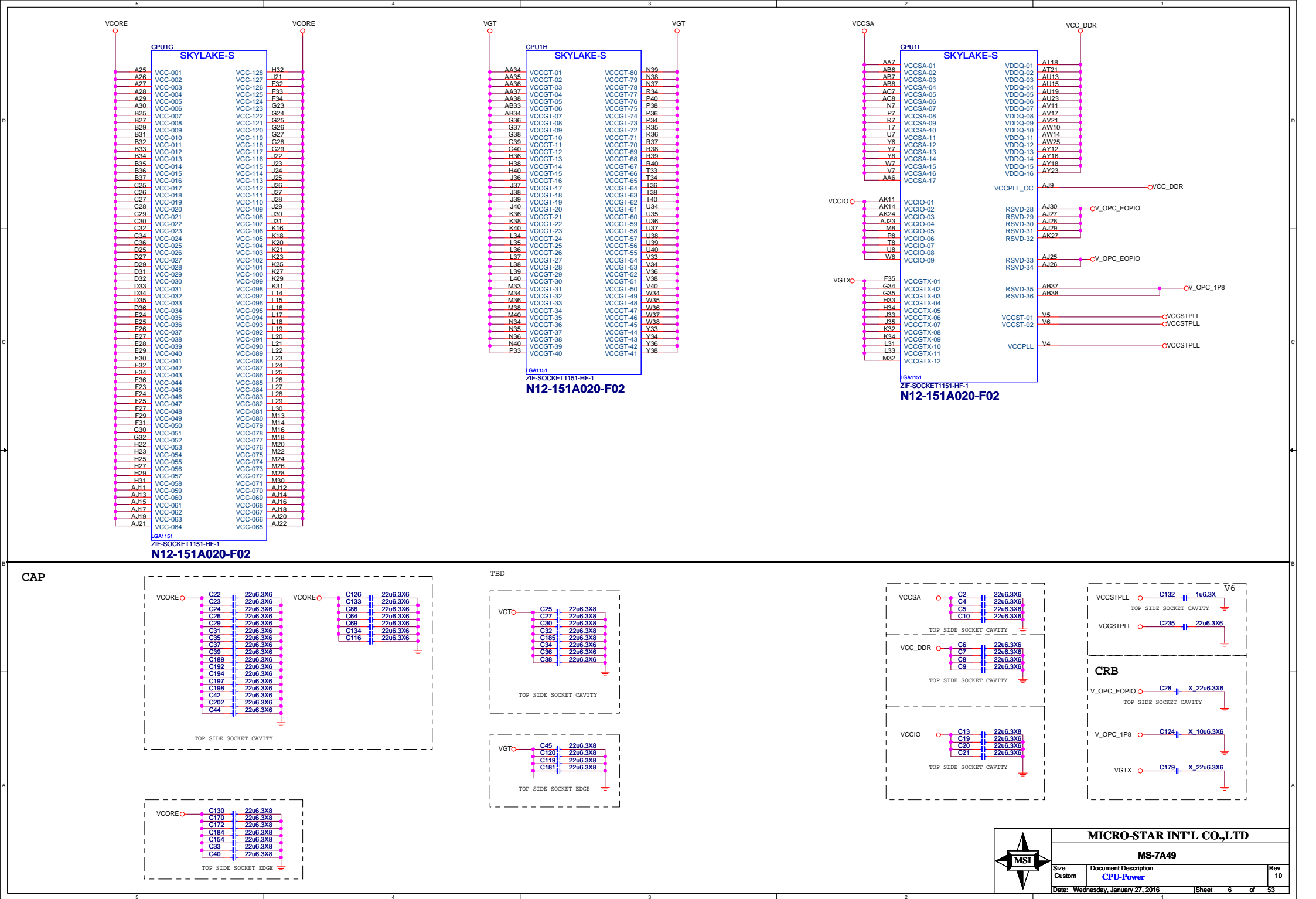
modify 2014.12.15

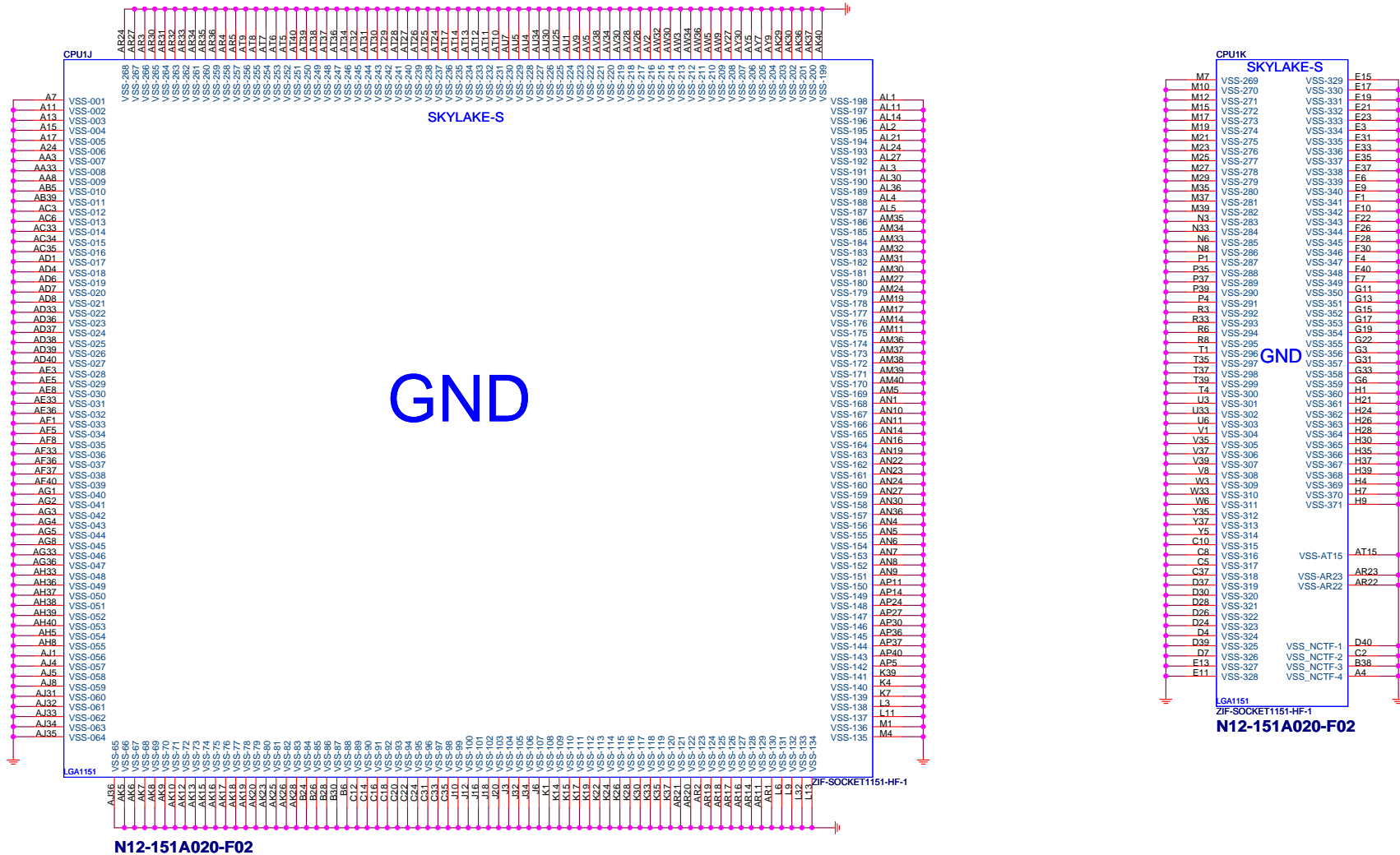


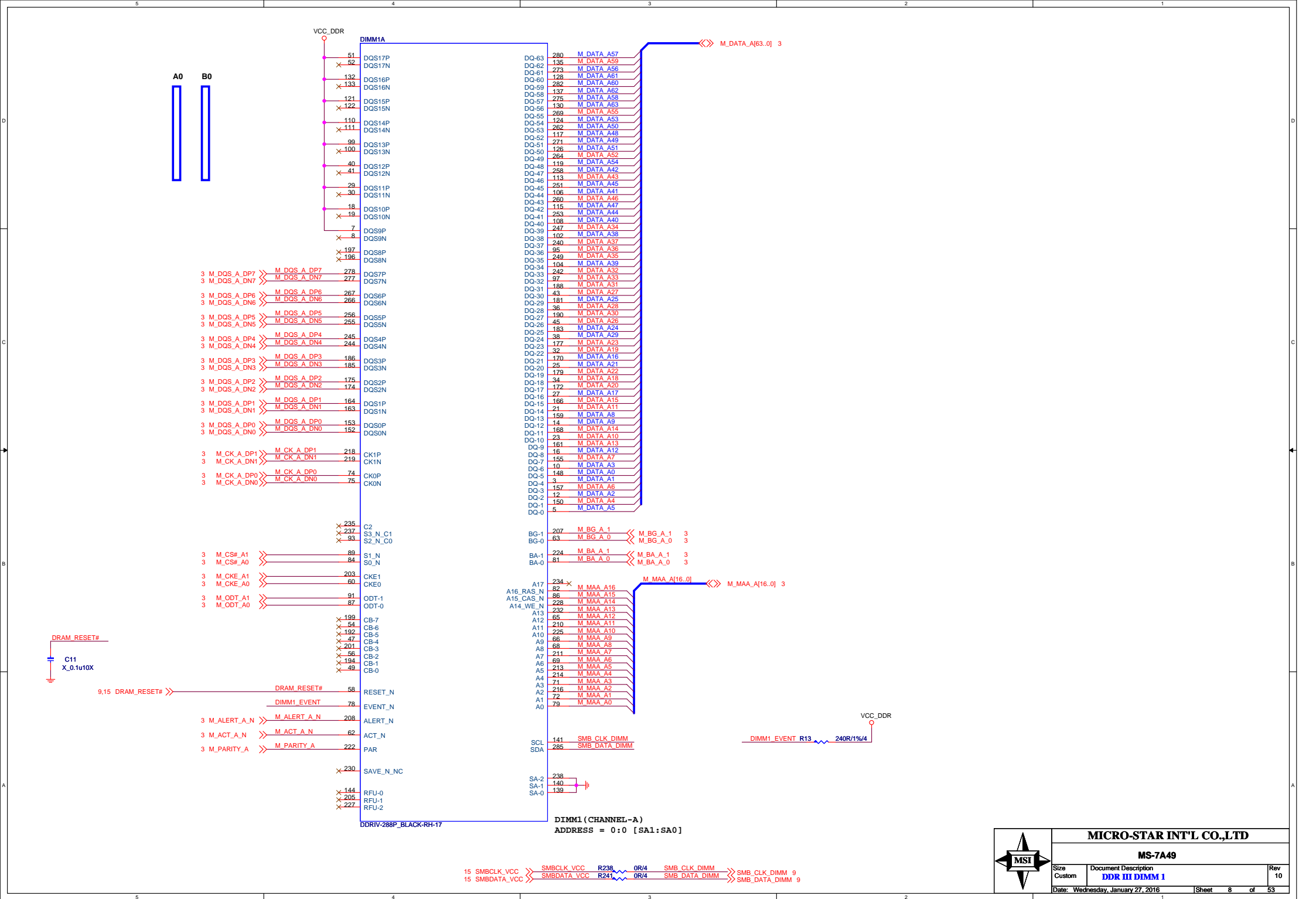
modify 2014.09.19

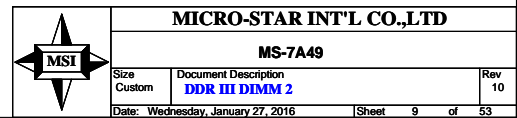
POWER DOWN

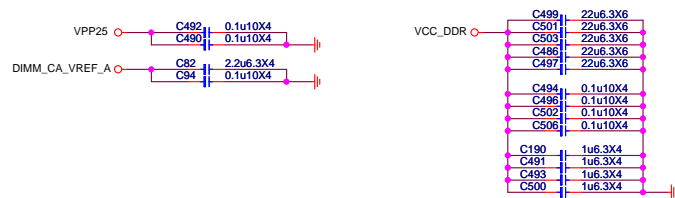
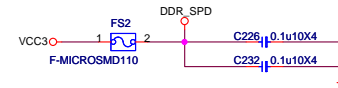
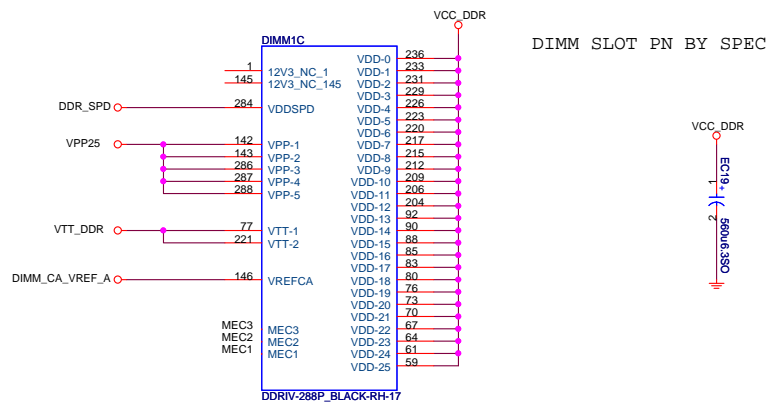




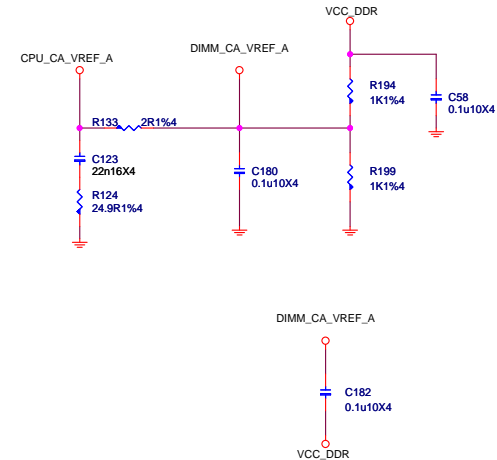
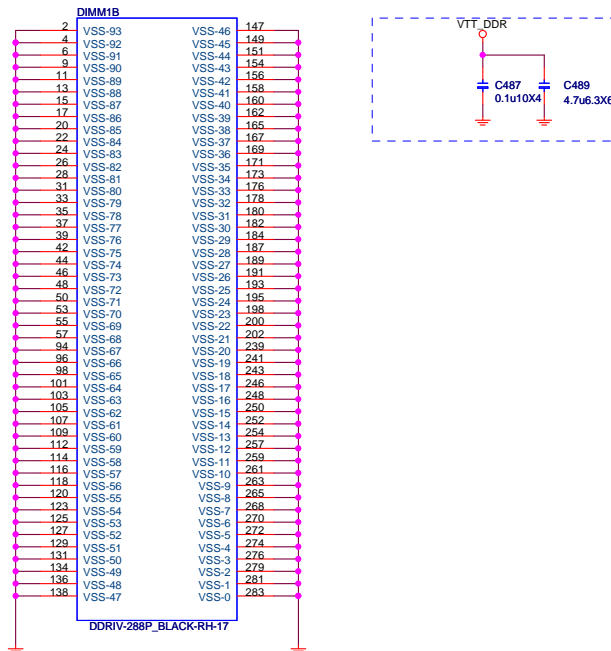








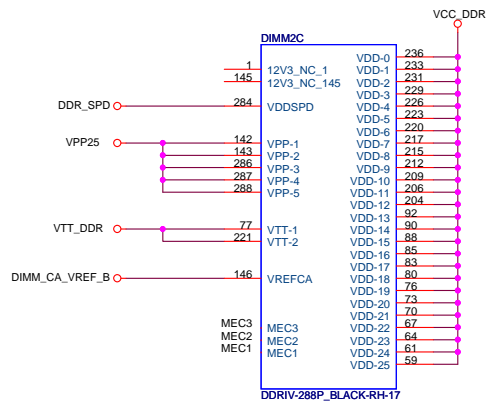
0.1uFxl per dimm



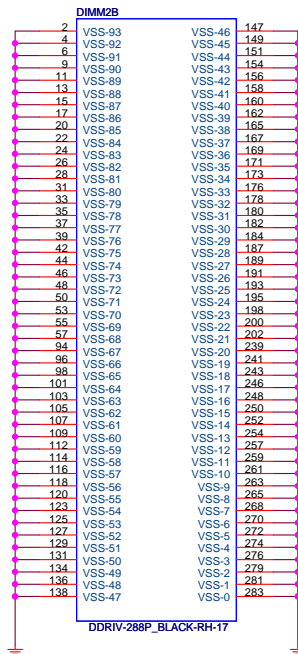
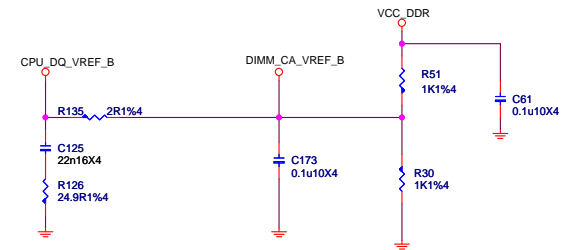
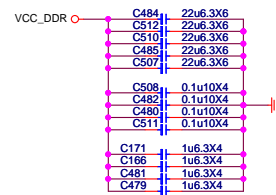
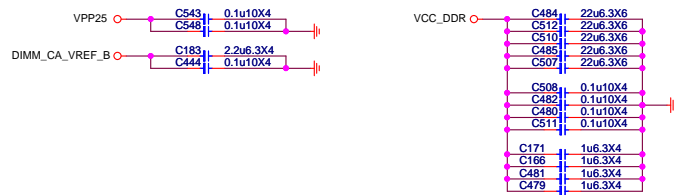
MICRO-STAR INT'L CO.,LTD

MS-7A49

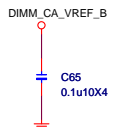
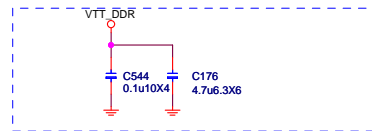
Size	Document Description	Rev
Custom	DDR4-POWER/GND-1	10
Date:	Wednesday, January 27, 2016	Sheet 10 of 53



Place close to DIMM2



0.1uFxl per dimm



H110:1-4
B150:1-6

PCH1A

SPT-H_PCH

USB 3.0

USB 2.0

PCIe/USB 3

DMi

B01-0H11005-I06

1 OF 12

H110:1-10
B150:1-12

USB2_COMP < 500 mil

H110 : PCIE 6 Port(Gen2)

B150 : PCIE 10 Port(Gen3)

B01-0H11005-I06

2 OF 10

GPP_E8/SATALED#

H110

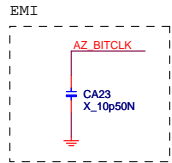
2014.09.05 check list



MICRO-STAR INT'L CO.,LTD

MS-7A49

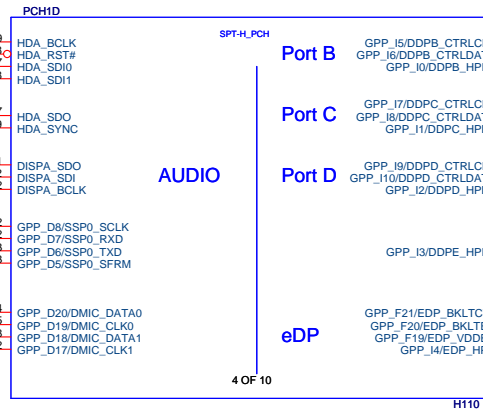
Size	Document Description	Rev
Custom	PCB-USB/PCIE/DMI/SATA	10
Date:	Wednesday, January 27, 2016	Sheet 12 of 53



26 AZ_BITCLK << AZ_BITCLK R449 33R AZ_BITCLK_LR BA9
26 AZ_RST# << AZ_RST# R510 33R AZ_RST#_R BD8
26 AZ_SDIN0 << AZ_SDIN0 R489 33R AZ_SYNC_R BE7
XBC8

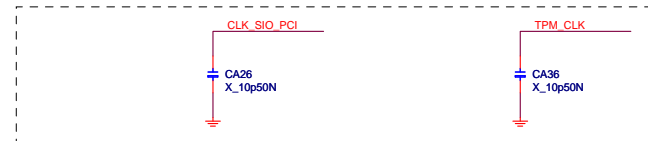
18 AZ_SDOUT_R << AZ_SDOUT_R R489 33R AZ_SYNC_R BE7
26 AZ_SYNC << AZ_SYNC R489 33R AZ_SYNC_R BE7
XBC8

5 PCH_CPU_AUD_SDO << R412 33R PCH_CPU_AUD_SDO_R AM1
5 PCH_CPU_AUD_SDI << R419 33R PCH_CPU_AUD_SDI_R AM2
5 PCH_CPU_AUD_SCLK << R419 33R PCH_CPU_AUD_SCLK_R AM2



B01-0H11005-I06

EMI

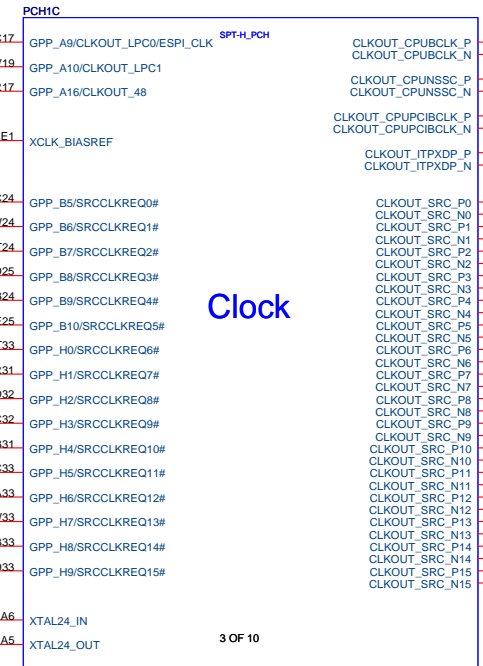


21 CLK_SIO_PCI << CLK_SIO_PCI R613 22R CLK_PCH_LPC0 BC17
46 TPM_CLK << R612 22R TPM_CLK_R AV19
TP18 CLKOUT 48M AR17

PCH_CLK5_1P0 << R339 2.7K/1% XCLK_BIASREF E1
XCLK_BIASREF < 500 mil

ASM1083 23 CLKREQ#1 << CLKREQ#1 BC24
CLKREQ#1 << CLKREQ#1 AW24
CLKREQ#2 << AT24
CLKREQ#3 << BD25
LAN 28 CLKREQ#4 << CLKREQ#4 BB24
CLKREQ#5 << BE25
CLKREQ#6 << AT33
CLKREQ#7 << AR31
CLKREQ#8 << BD32
CLKREQ#9 << BC32
CLKREQ#10 << BB31
CLKREQ#11 << BC33
CLKREQ#12 << AW33
CLKREQ#14 << BB33
CLKREQ#15 << BD33

XTAL24M_PCH_IN A6
XTAL24M_PCH_OUT A5



B01-0H11005-I06

3 OF 10

H110

G2 PCH_CPU_BCLK_DP << PCH_CPU_BCLK_DP 5 100M
H2 PCH_CPU_BCLK_DN << PCH_CPU_BCLK_DN 5
G1 PCH_CPU_NSSC_CLK_DP << PCH_CPU_NSSC_CLK_DP 5 24M
F1 PCH_CPU_NSSC_CLK_DN << PCH_CPU_NSSC_CLK_DN 5
J2 PCH_CPU_PCIE_DP << PCH_CPU_PCIE_DP 5 100M
J1 PCH_CPU_PCIE_DN << PCH_CPU_PCIE_DN 5
L2 << <<
L1 << <<

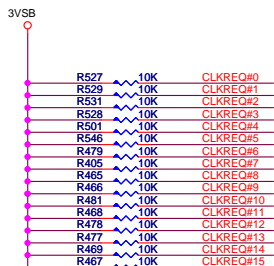
N8 << CK_SLOT2_DP 20
N7 << CK_SLOT2_DN 20
L5 << CK_ASM1083_DP 23
L7 << CK_ASM1083_DN 23
D3 << <<
G4 << <<
E5 << CK_SLOT1_DP 19
E6 << CK_SLOT1_DN 19
D5 << CK_PE_LAN 28
D7 << CK_PE_LAN# 28
D8 << <<
D9 << <<
R7 << <<
R8 << <<
U7 << <<
U5 << <<
W11 << <<
W10 << <<
N3 << <<
P2 << <<
P3 << <<
R4 << <<
R3 << <<
U3 << <<
U2 << <<
Y5 << <<
W7 << <<
R2 << <<
P1 << <<
R11 << <<
R13 << <<

DVI_DDPC_CTRLCLK R410 2.2K
DVI_DDPC_CTRLDATA R415 2.2K
DP_DDPC_CTRLCLK R523 2.2K
DP_DDPC_CTRLDATA R492 2.2K

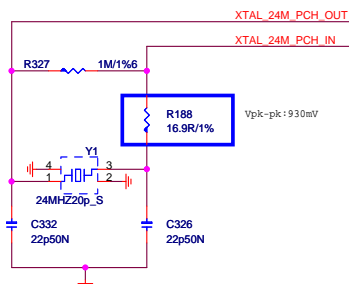
DDI interface Disable
no connect

Port C DVI

Port D DisplayPort



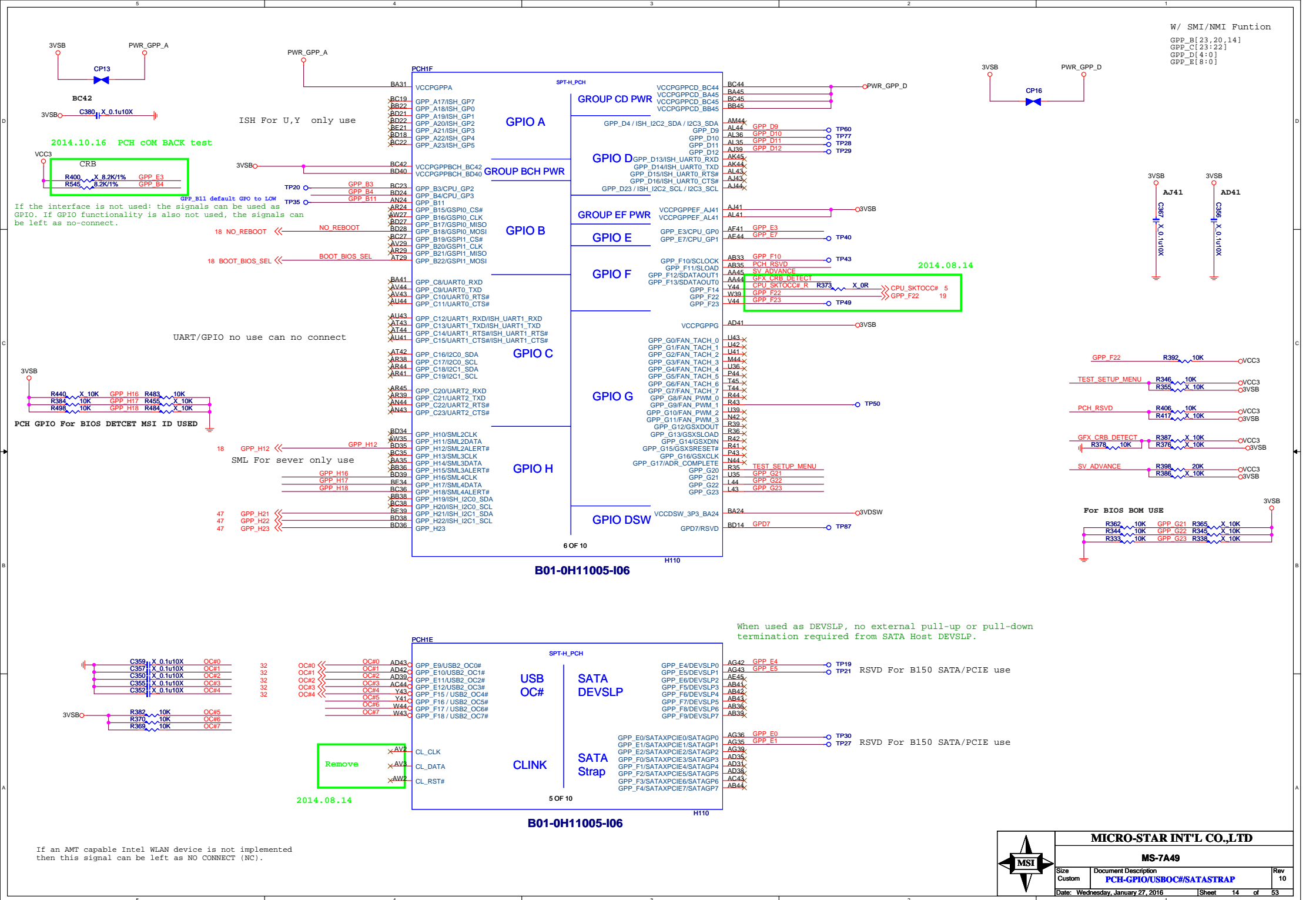
Contact to SLOT Pin B12
for support L1 PM Substates
ME also can disable this function.

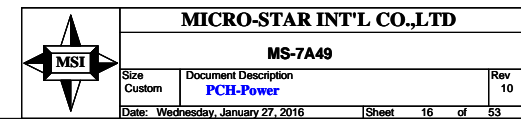
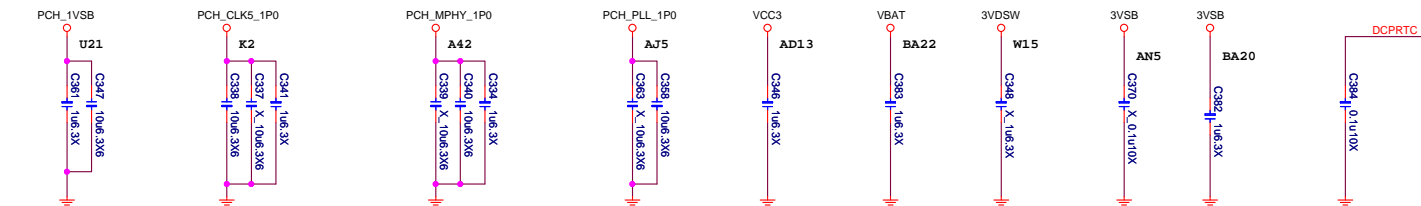


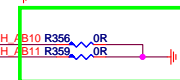
MICRO-STAR INT'L CO.,LTD

MS-7A49

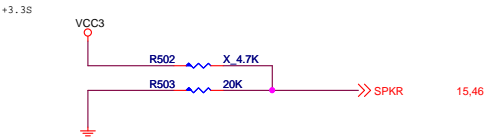
Size	Document Description	Rev
Custom	PCH-Audio/Display/Clock	10
Date: Wednesday, January 27, 2016	Sheet 13 of 53	





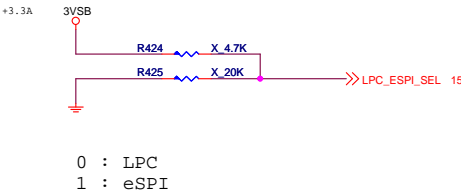


TOP Swap



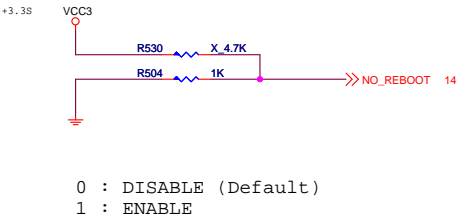
Internal pull-down 20K is disabled after PLTRST#

LPC eSPI Mode



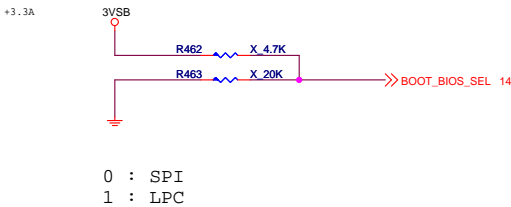
Internal pull-down 20K is disabled after RSMRST

No Reboot



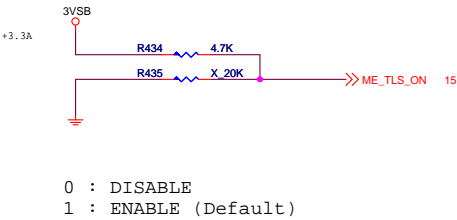
Internal pull-down 20K is disabled after PLTRST#

Boot BIOS



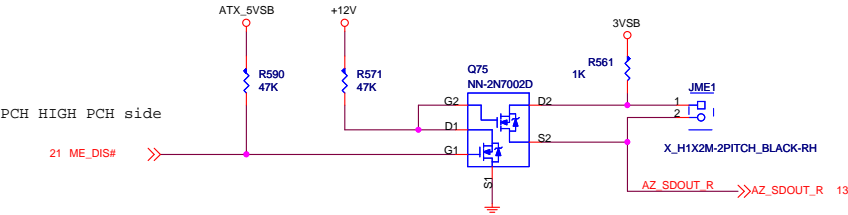
Internal pull-down 20K is disabled after PLTRST

AMT and SBA with confidentiality

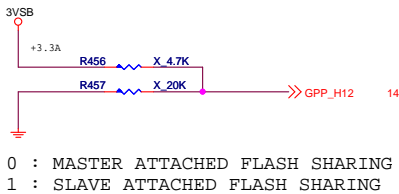


Internal pull-down 20K is disabled after RSMRST

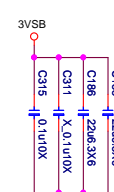
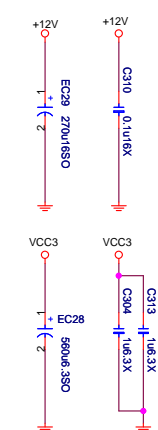
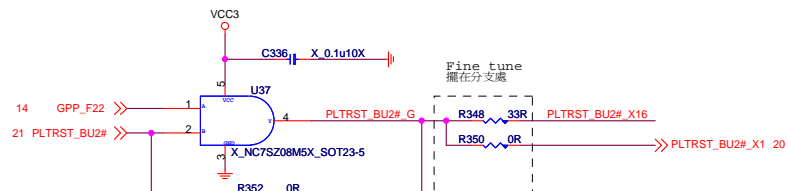
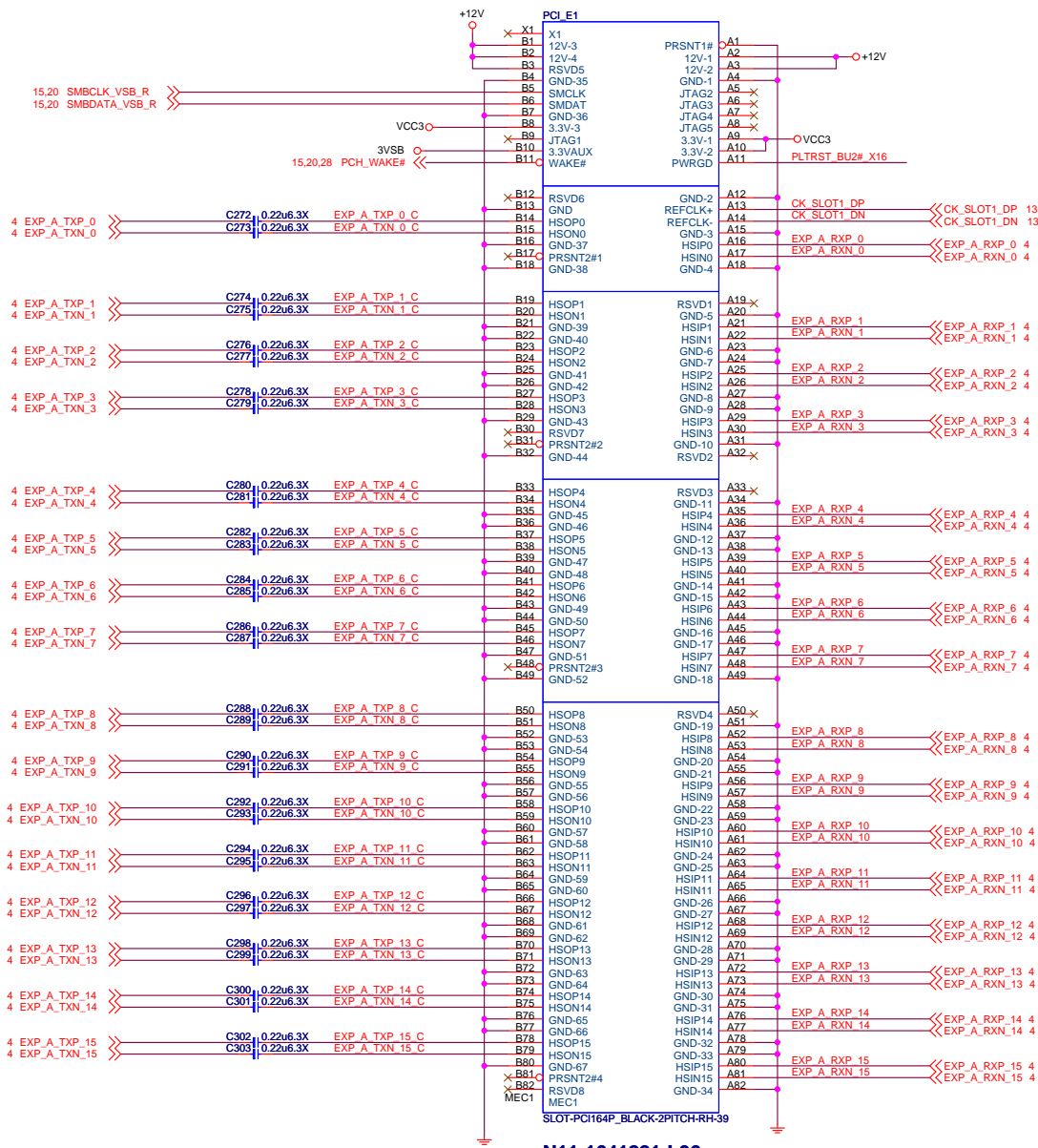
HDA_SDO

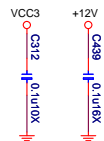
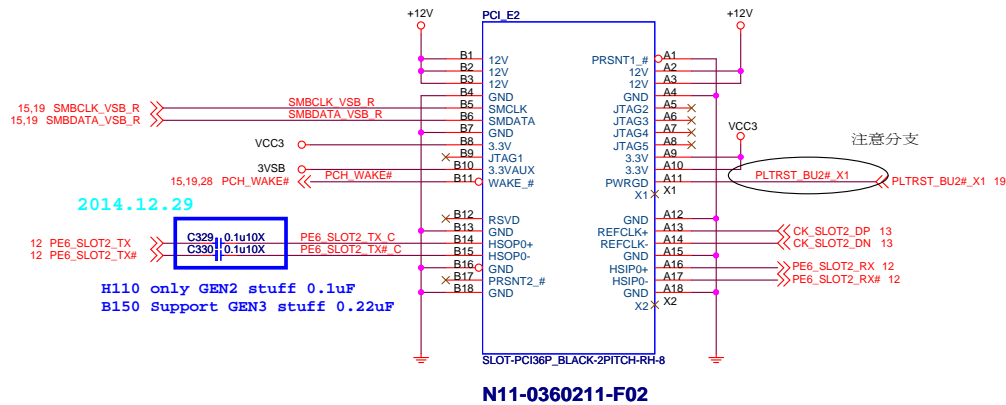


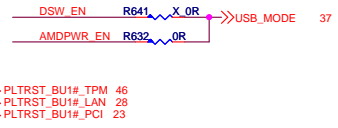
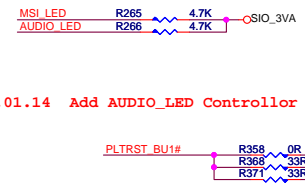
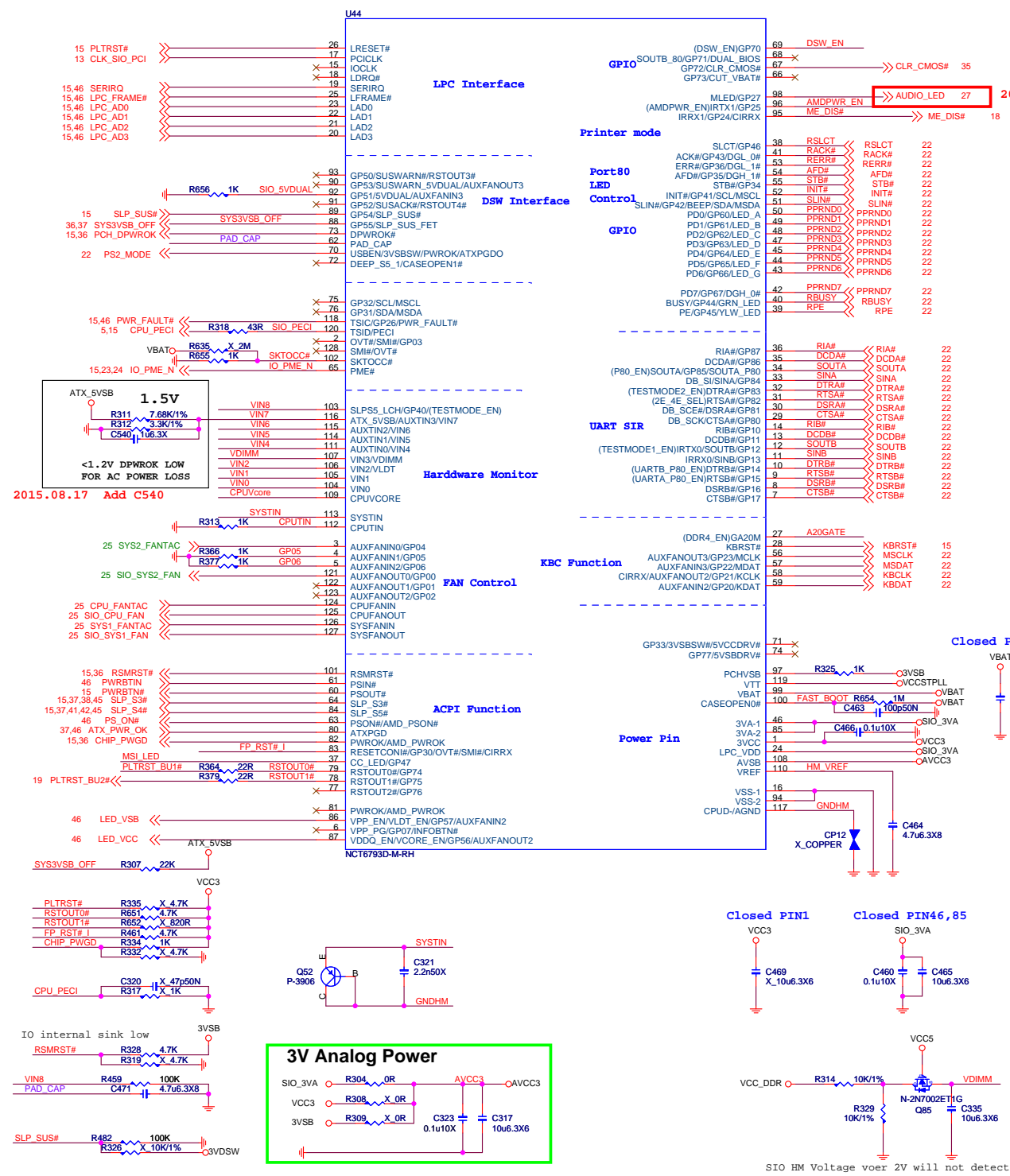
ESPI FLASH SHARING MODE



Internal pull-down 20K is disabled after RSMRST





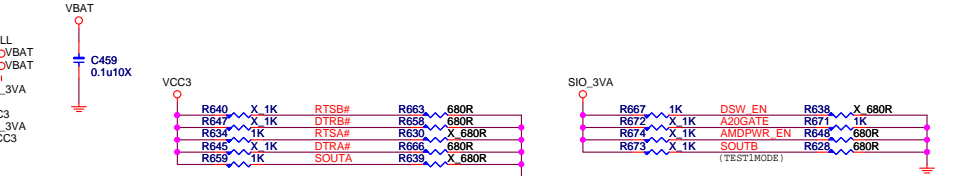


POWER ON STRAPPING PIN FOR NCT6792

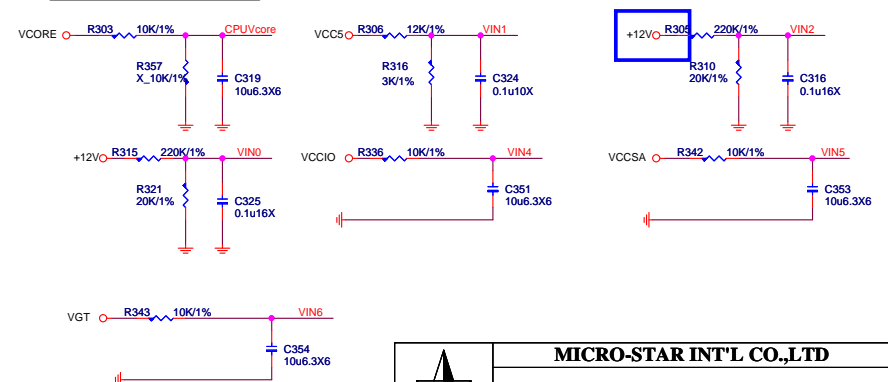
PIN	6792 NAME	Circuit NAME	0	1	Strap Point
	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO

Closed PIN99



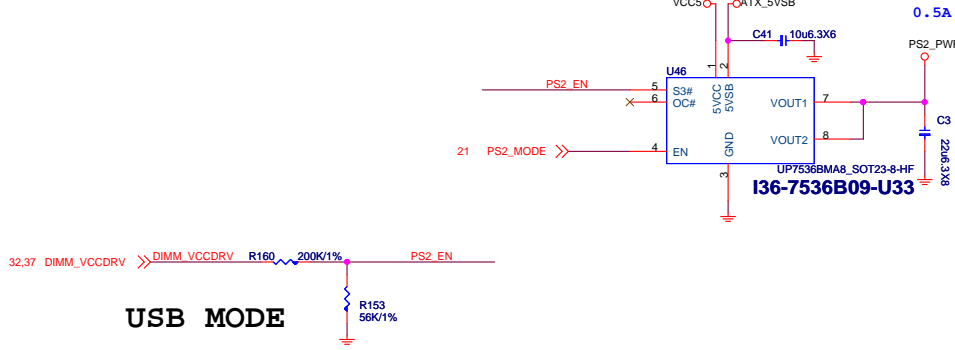
HW Monitor - Voltage



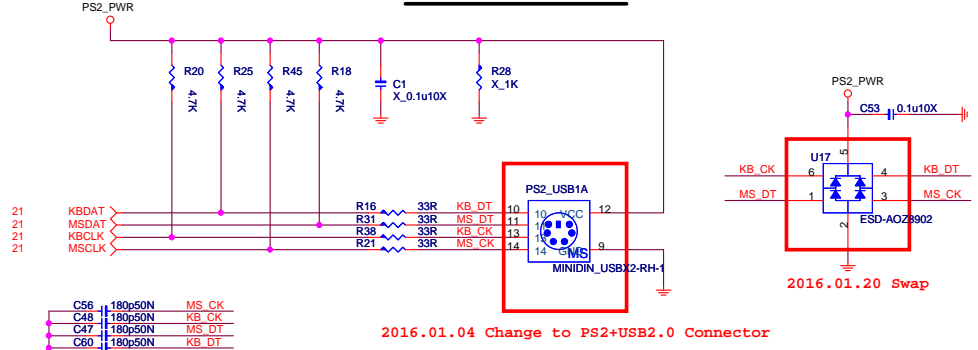
MICRO-STAR INT'L CO.,LTD
MS-7A49
Size Custom Document Description **SIO-NCT6793D** Rev 10
Date: Wednesday, January 27, 2016 Sheet 21 of 53

SIO HM Voltage voer 2V will not detect

PS2 MODE

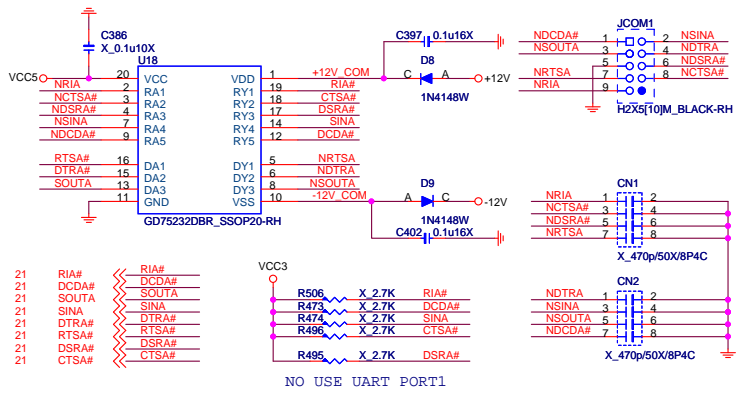


PS2 Connector

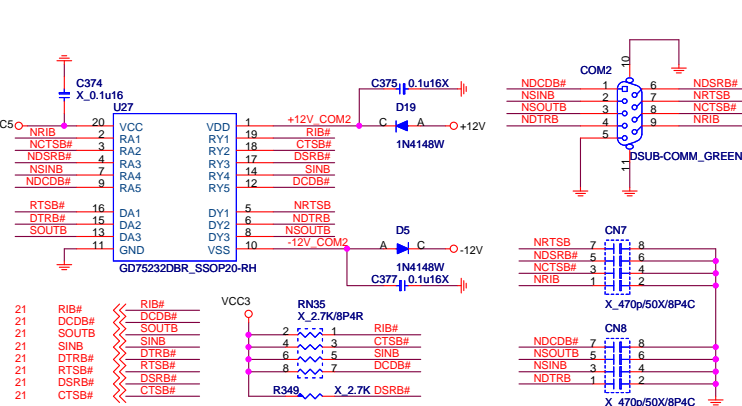


USB MODE

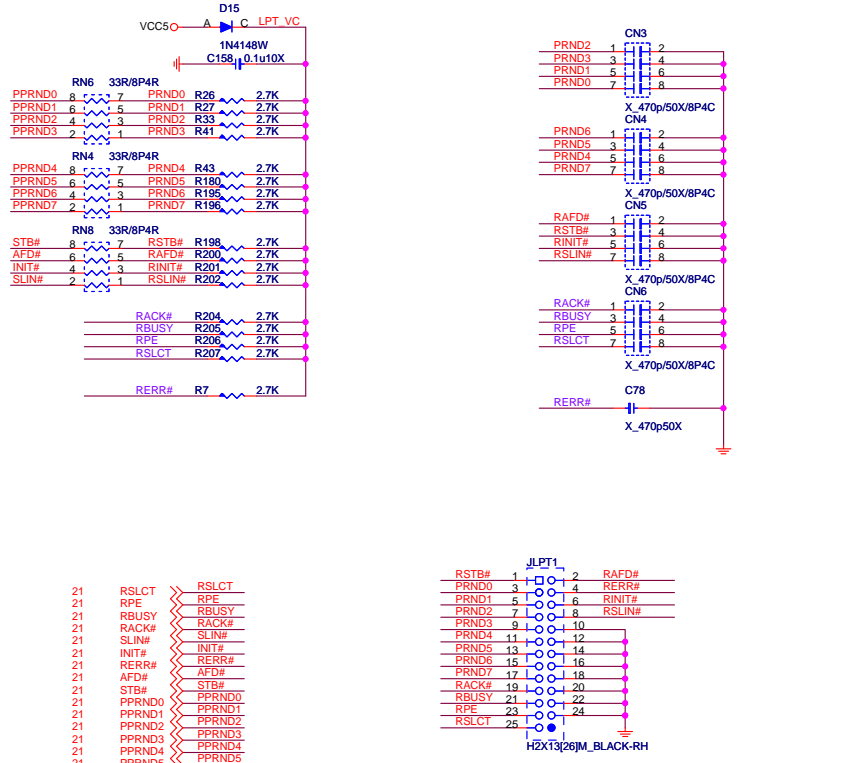
SERIAL PORT 1



SERIAL PORT 2

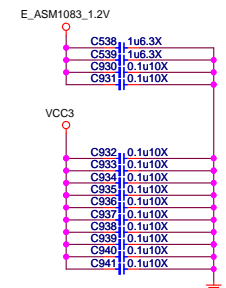
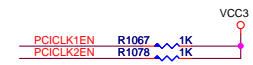
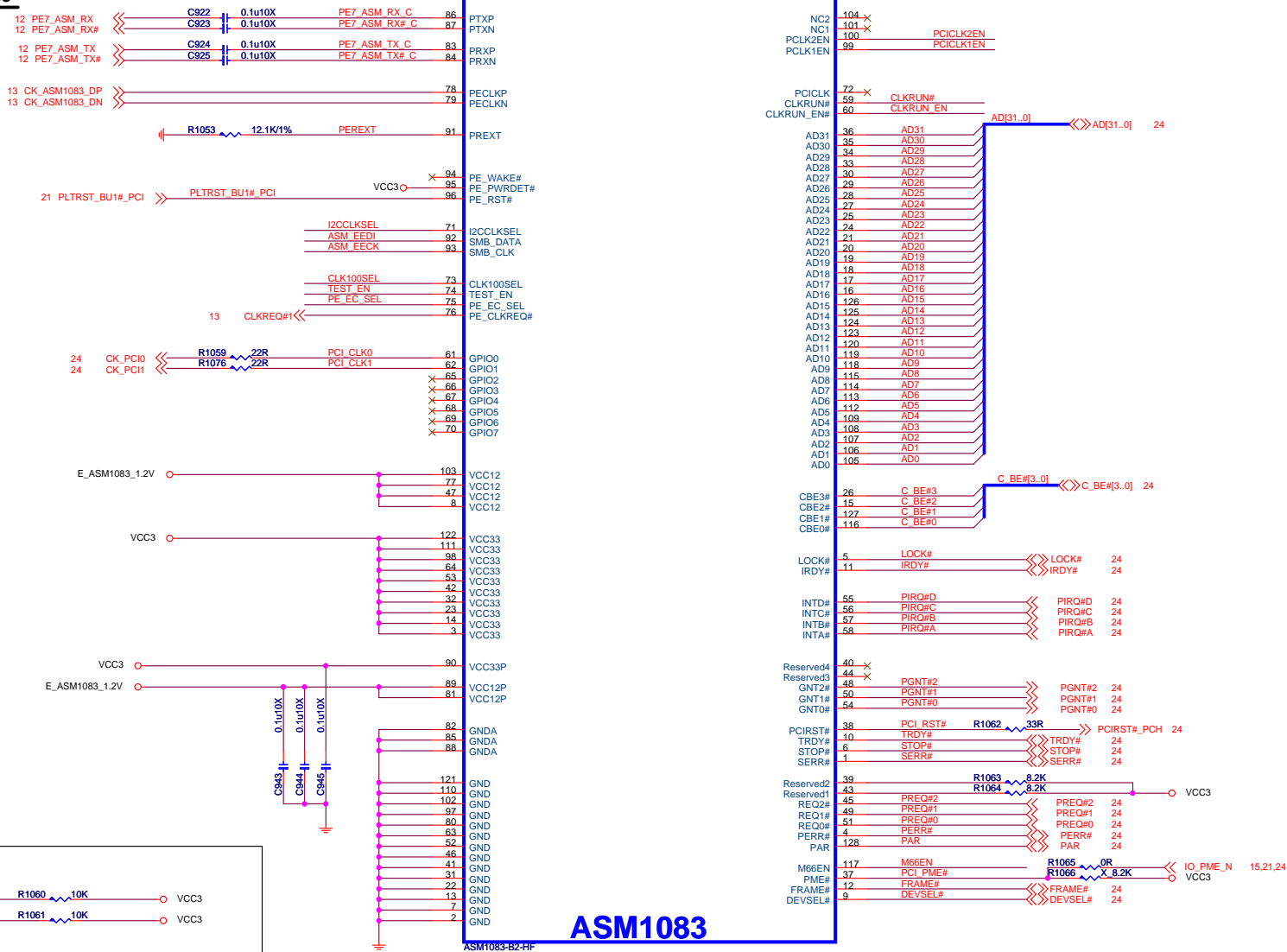


JLPT1 PORT

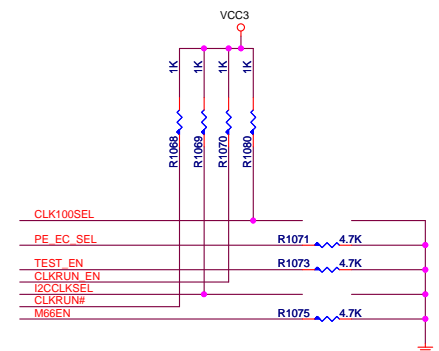


N31-2131151-H06 : 2.0mm
N31-2131131-H06 : 2.54mm

Title			SIO-NCT6793D
Size	Document Number	Rev	
Custom	M45-7A49	10	
Date:	Wednesday, January 27, 2016	Sheet	22 of 53

ASM1083

H/W Strapping



CLK100SEL-
 "H" for PECLK input only
 "L" for PECLK & PCICLK input

PE_EC_SEL-
 "H" for Express Card mode
 "L" for PCIe Riser Card mode

TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

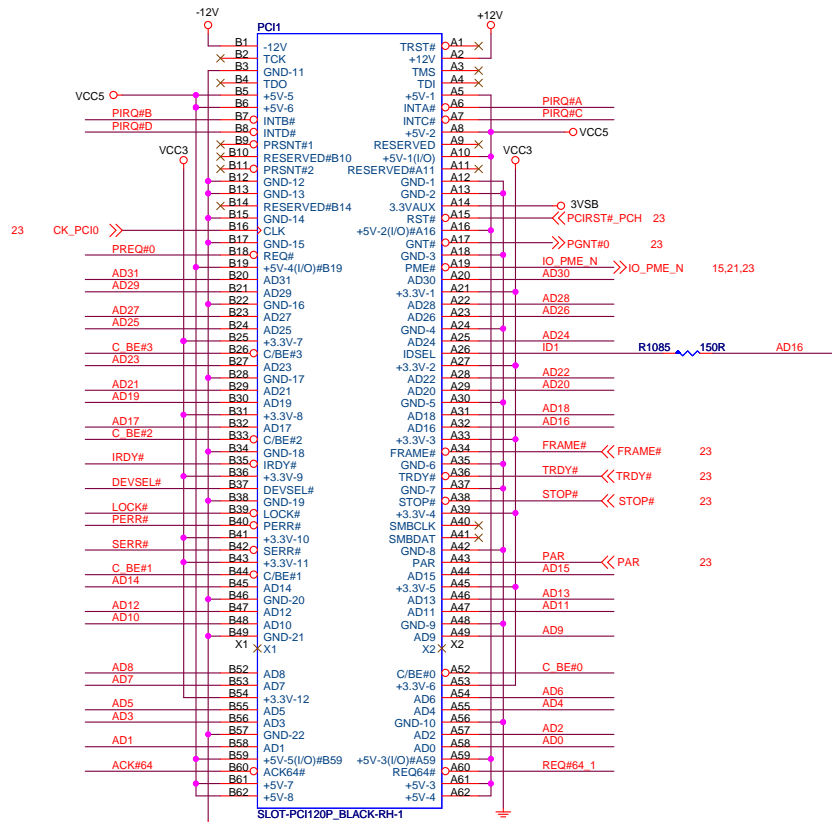
```
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK
```



MICRO-STAR INT'L CO.,LTD

MS-7A49

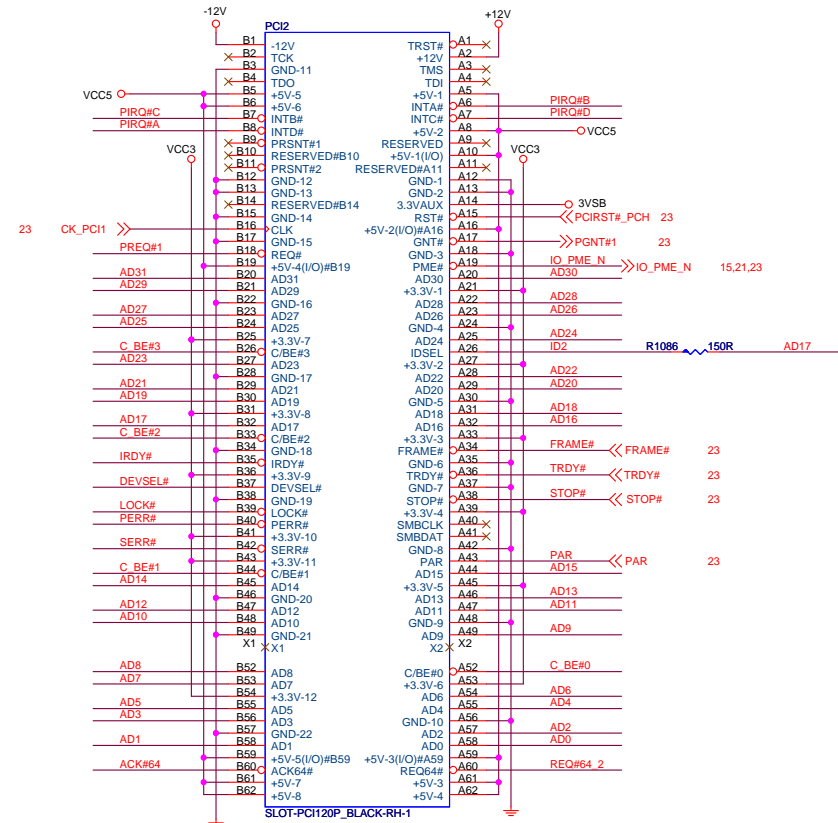
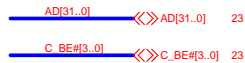
Size Custom	Document Description ASM1083 PCI Bri.	Rev 10
Date: Wednesday, January 27, 2016		Sheet 23 of 53



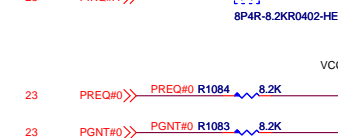
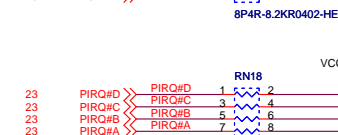
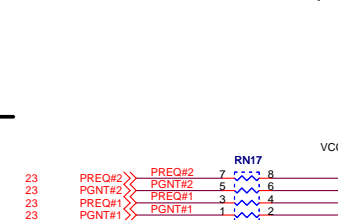
```

IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

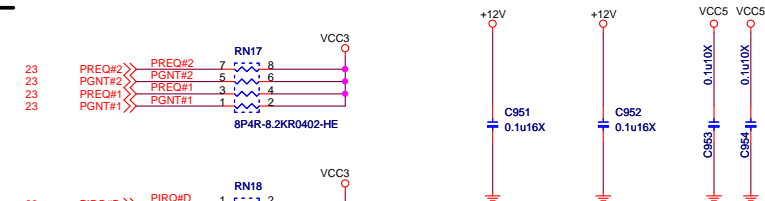
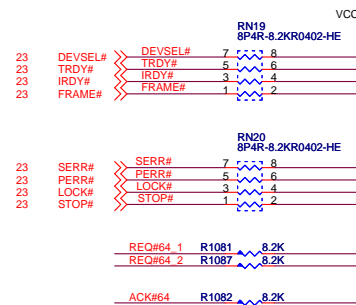
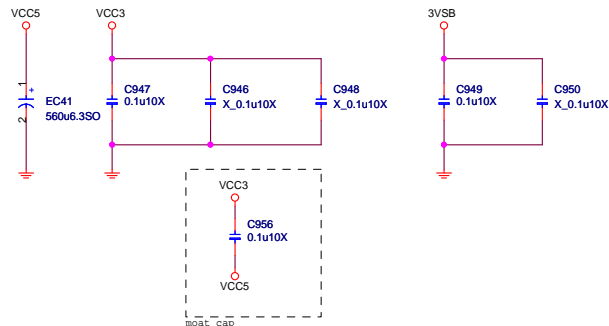
```



```
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B
```



PCI PULL-UP / DOWN RESISTORS

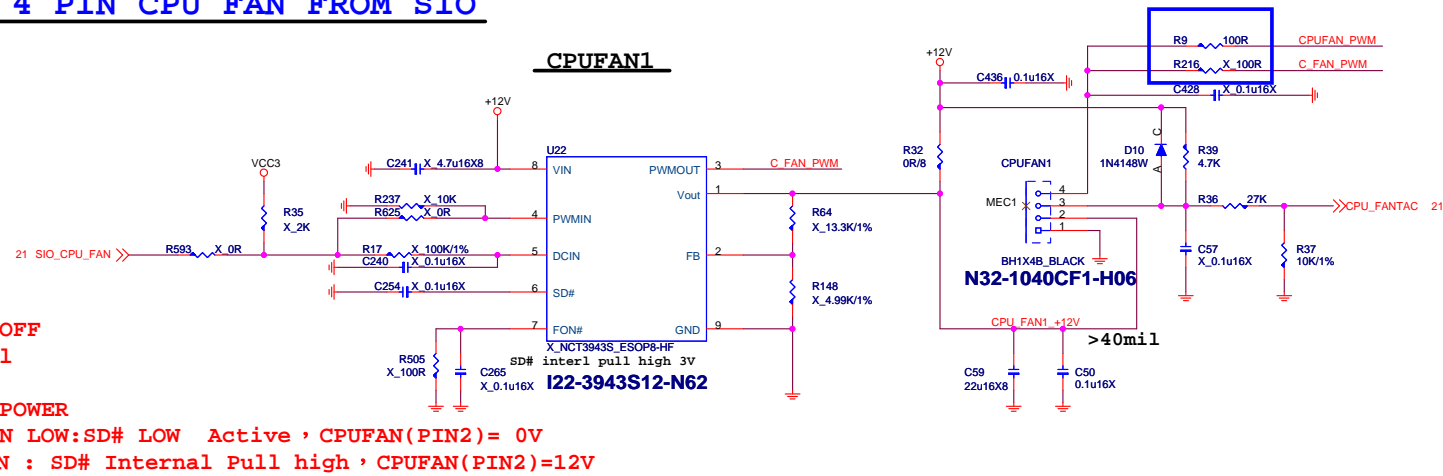


MICRO-STAR INT'L CO.,LTD

MS-7A49

Size Custom	Document Description PCIx1 Slots	Rev 10
Date: Wednesday, January 27, 2016		Sheet 24 of 53

Type G : 4 PIN CPU FAN FROM SIO



CPUFAN_PWR_OFF

GPIO Control

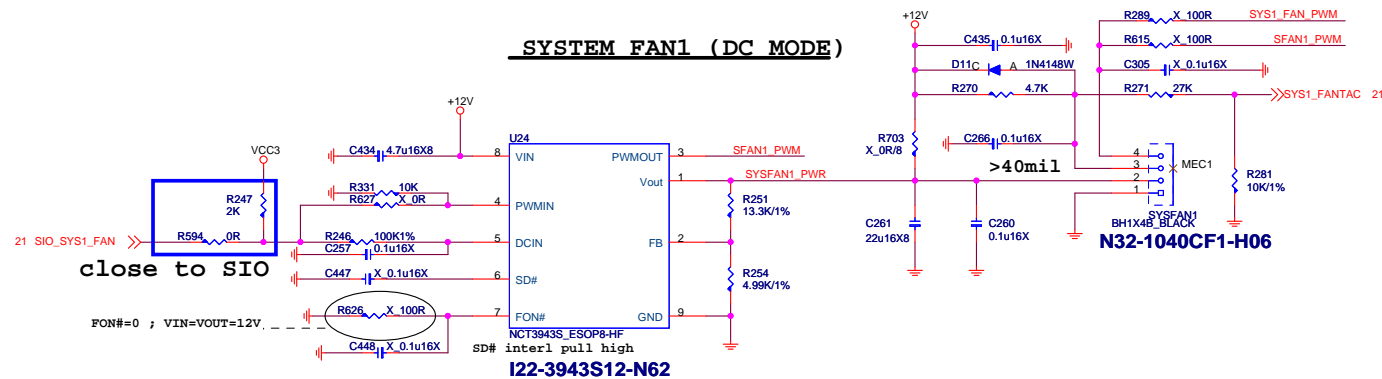
Deafult GPI

If USE CUT POWER

1.OPEN DRAIN LOW:SD# LOW Active , CPUFAN(PIN2)= 0V

2.OPEN DRAIN : SD# Internal Pull high , CPUFAN(PIN2)=12V

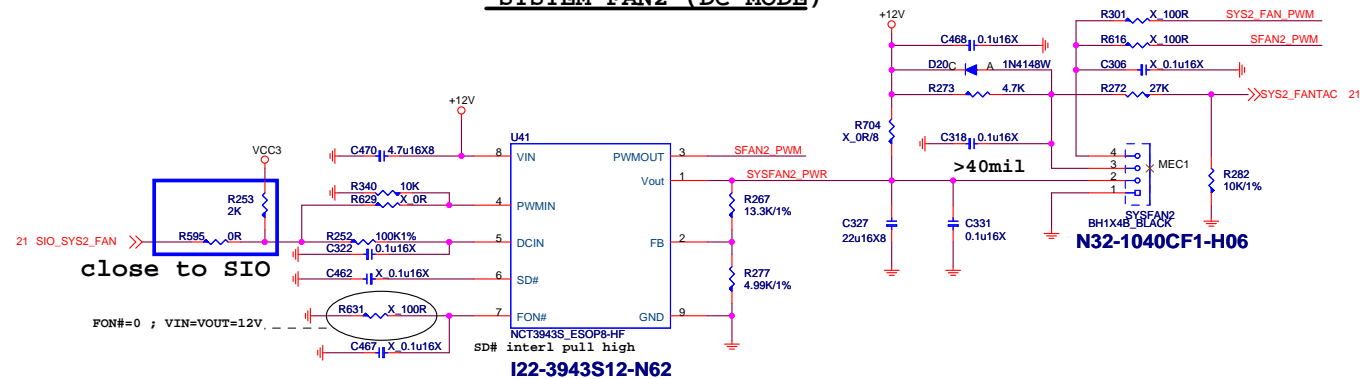
Type H : 4 PIN SYS FAN FROM SIO



close to SIO

FON#=0 ; VIN=VOUT=12V

SYSTEM FAN2 (DC MODE)



close to SIO

FON#=0 ; VIN=VOUT=12V

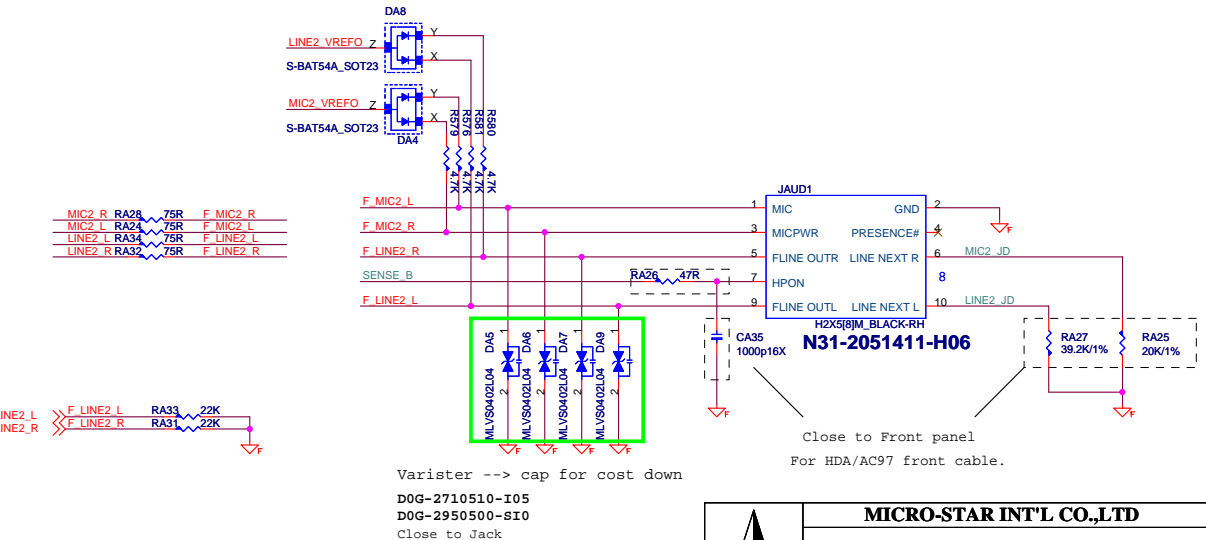
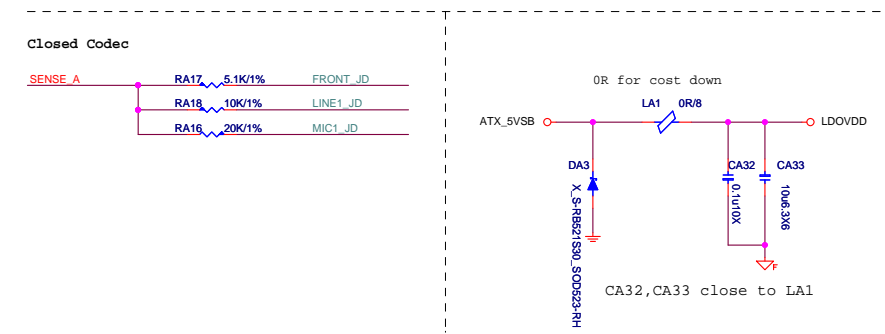
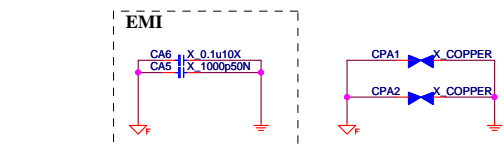
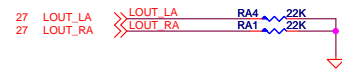
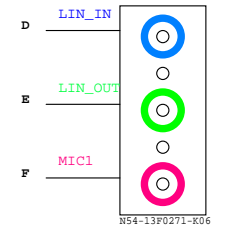
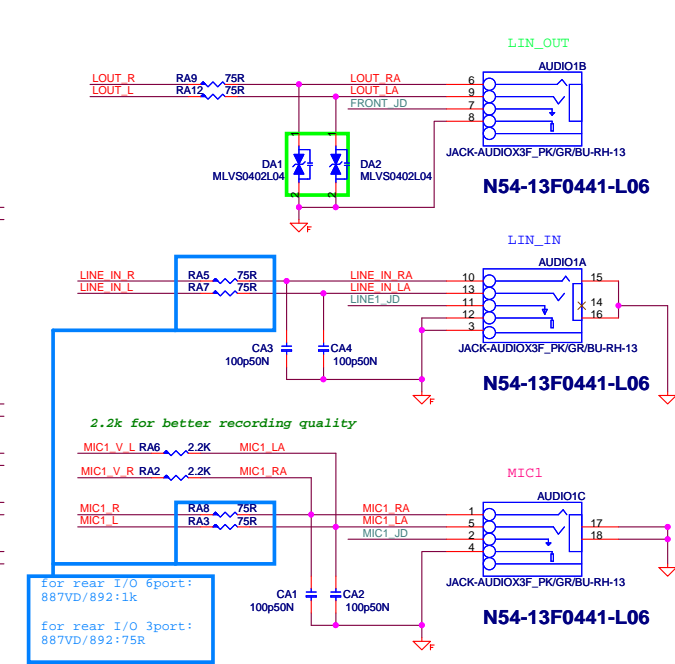
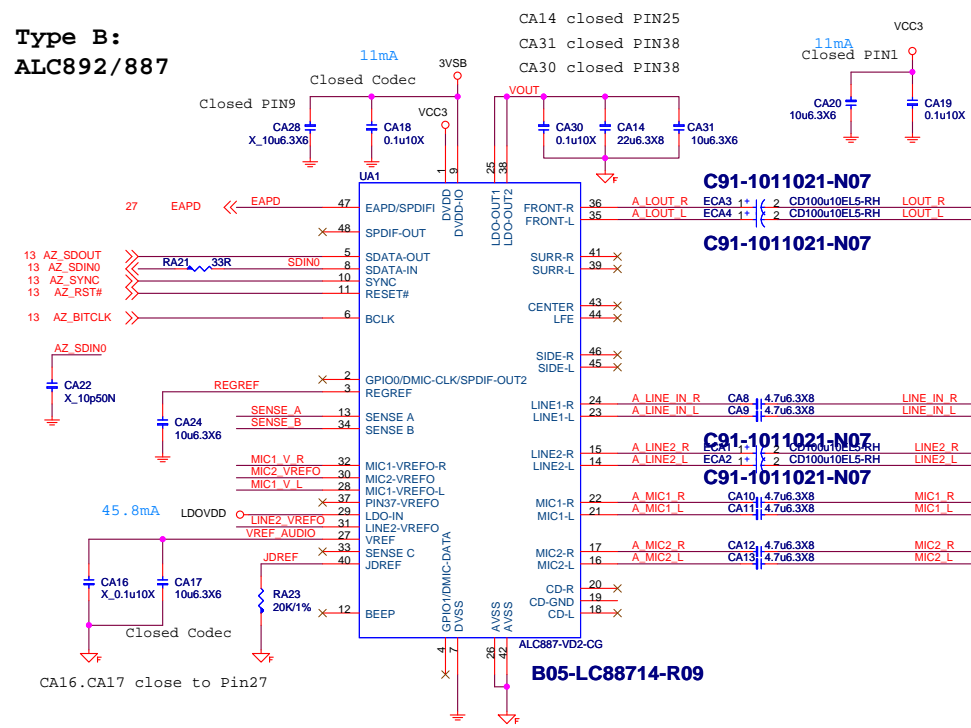


MICRO-STAR INT'L CO.,LTD

MS-7A49

Size	Document Description	Rev
Custom	FAN CONTROLLER	10
Date: Wednesday, January 27, 2016	Sheet 25 of 53	

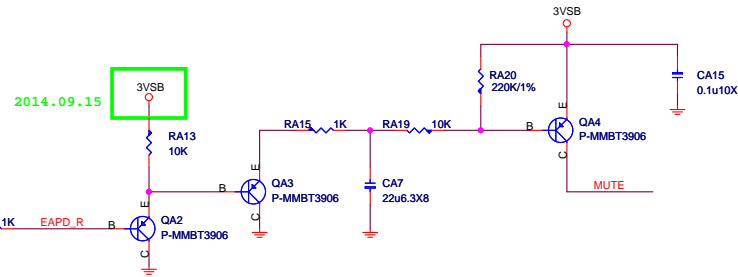
Type B:
ALC892/887



MICRO-STAR INT'L CO.,LTD			
MS-7A49			
Size Custom	Document Description AUDIO - ALC892/887		Rev 10
Date: Wednesday, January 27, 2016		Sheet 26 of	53

Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

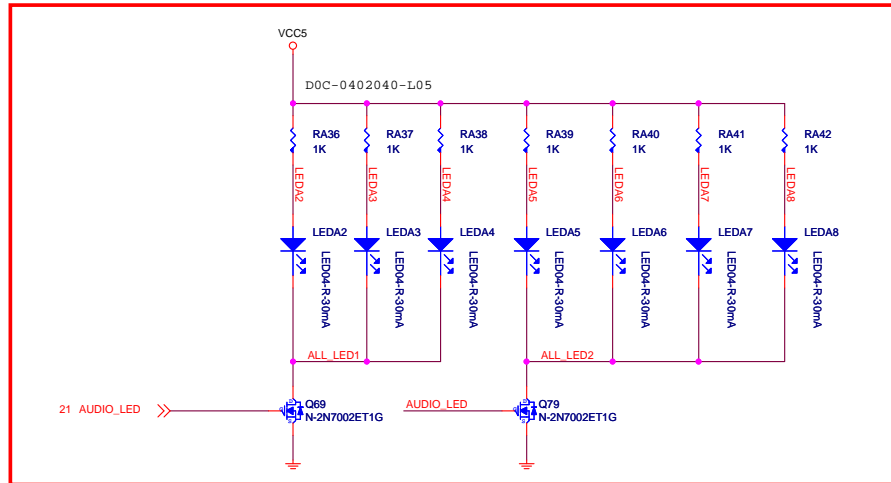


Digital

Analog



AUDIO LED MOAT



2016.01.14 Add AUDIO_LED Controller

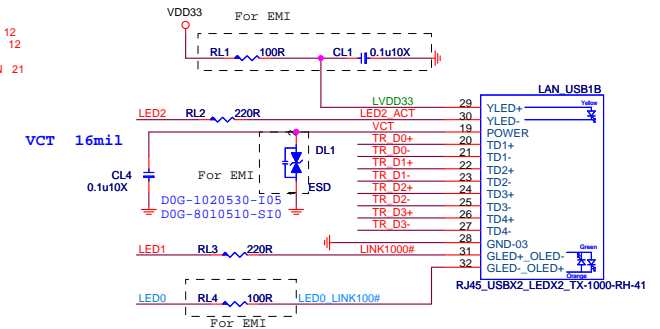
History:

2014/02/13: stuff de-pop circuit of Line out & HP out.

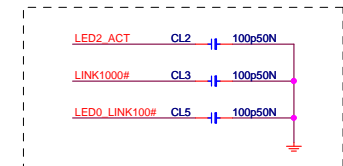
RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

LAN Connector

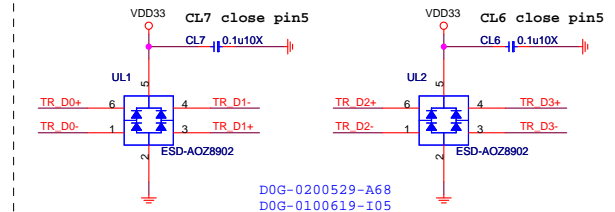


For EMI
2015.06.22



ESD Protect

UL2&UL3 close to connector



D0G-0200529-A68
D0G-0100619-I05

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



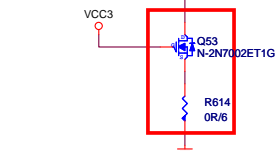
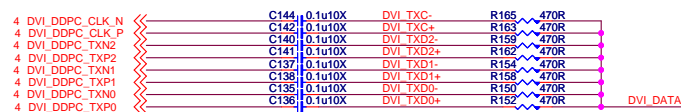
MICRO-STAR INT'L CO.,LTD

MS-7A49

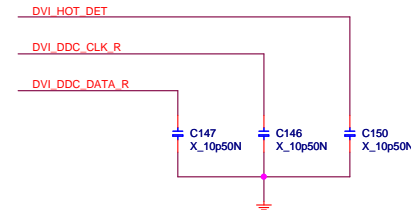
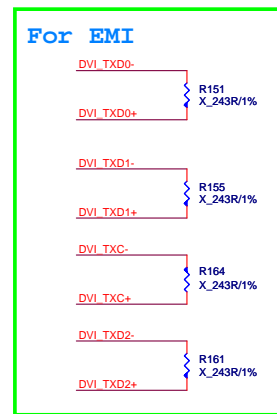
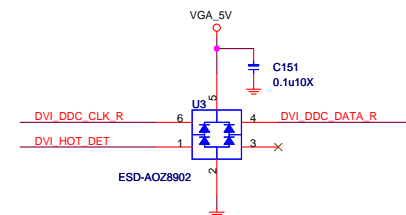
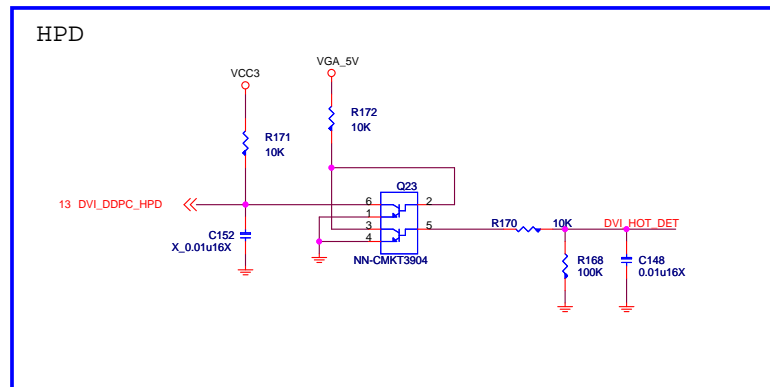
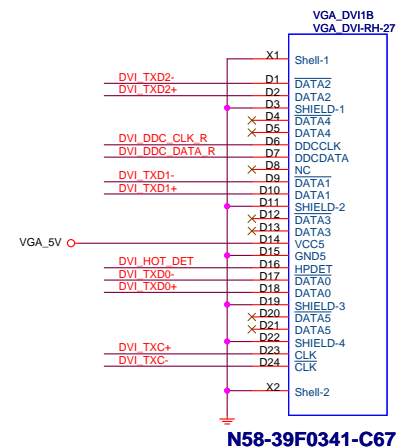
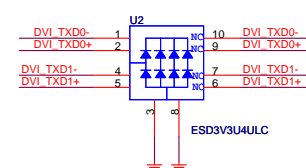
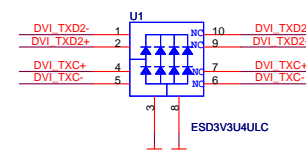
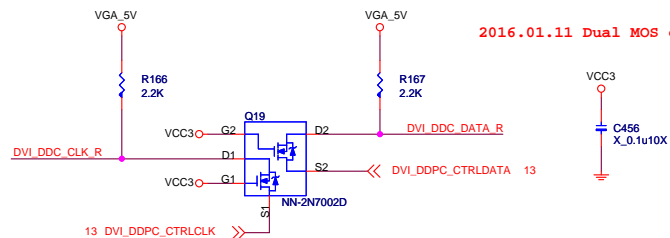
Size	Document Description	Rev
Custom	LAN - RTL8111H	10
Date: Wednesday, January 27, 2016	Sheet 28 of 53	

DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



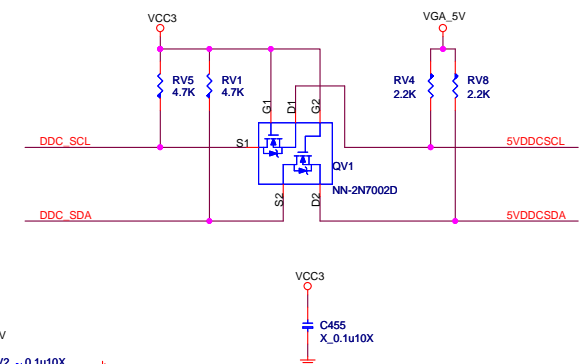
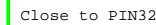
2016.01.11 Dual MOS change to single MOS, reduce CM noise by EMI Suggestion



If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



2015.01.09
For SA test fail



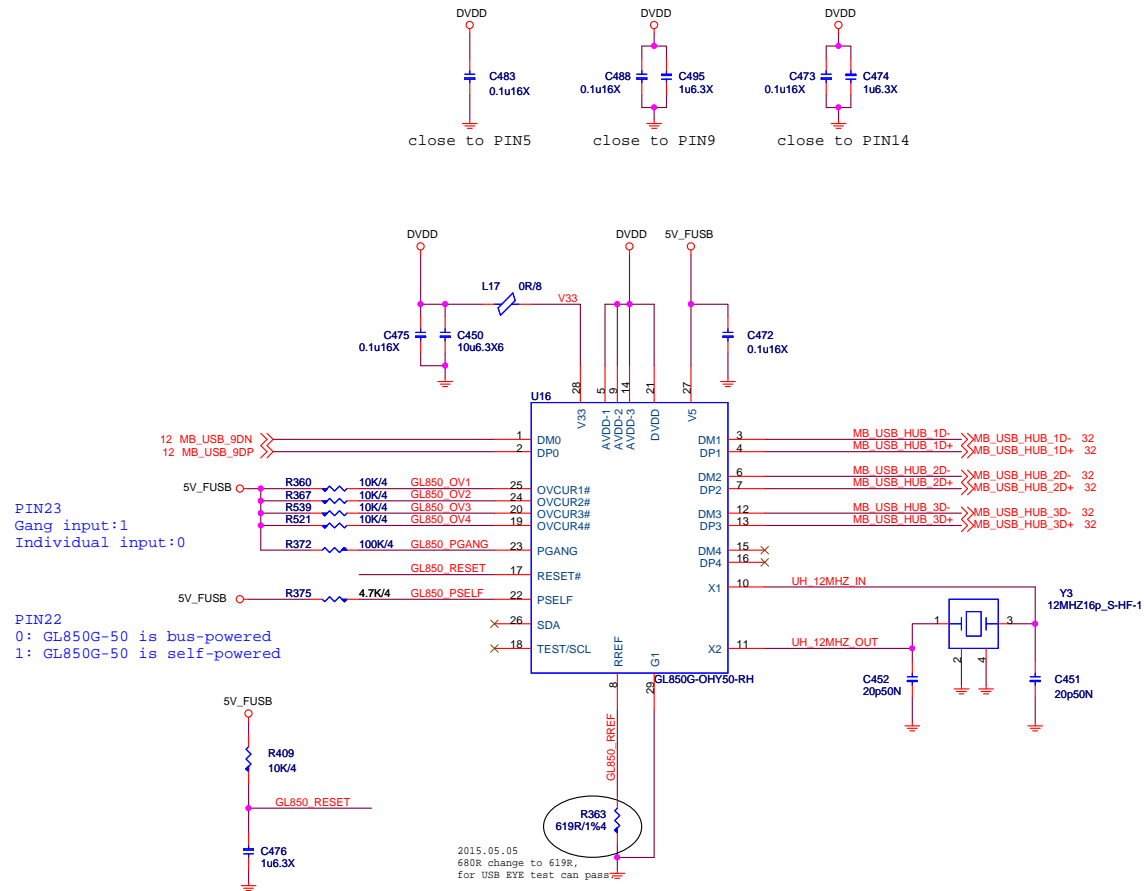
MICRO-STAR INT'L CO.,LTD

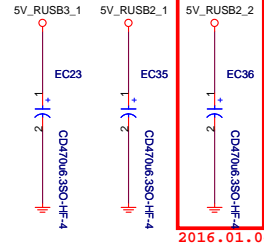
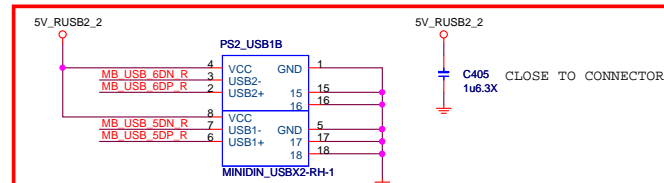
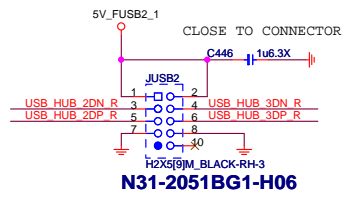
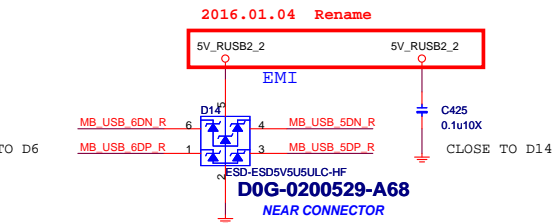
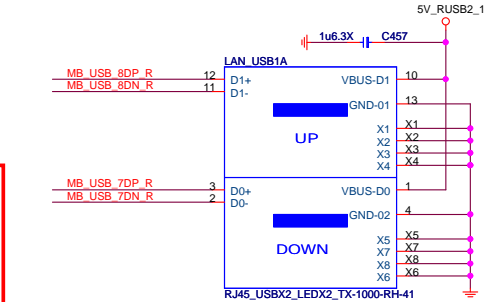
MS-7A49

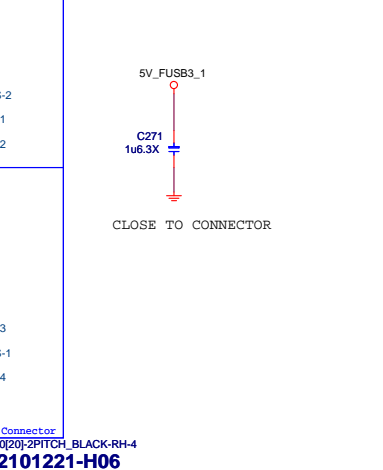
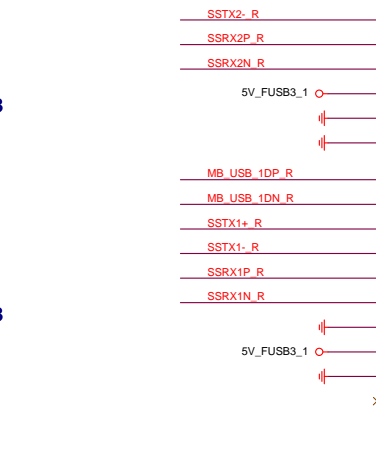
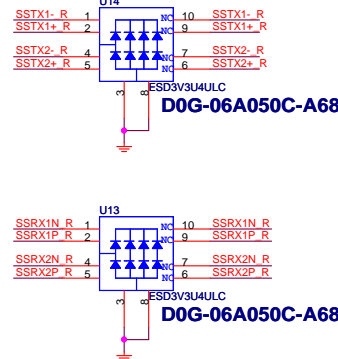
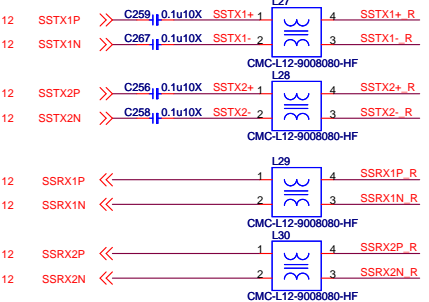
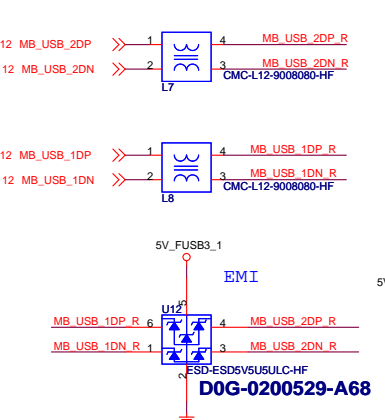
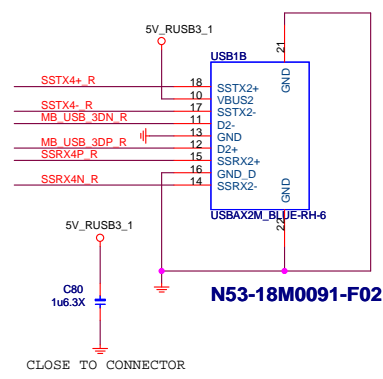
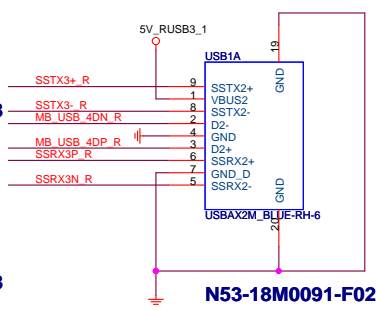
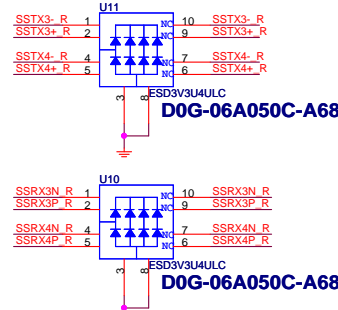
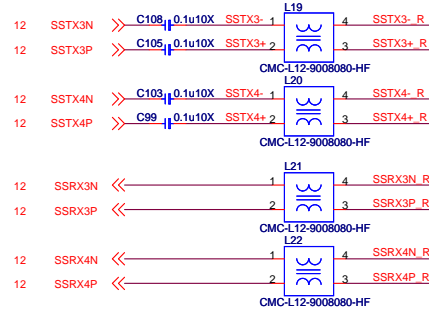
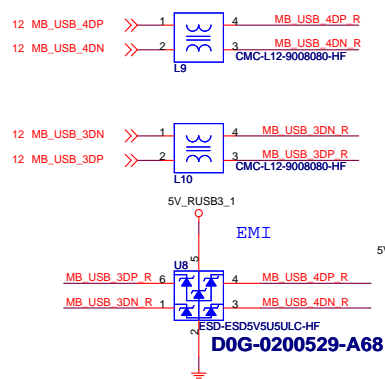
Size Custom	Document Description VGA - ITE6515	Rev 10
Date: Wednesday, January 27, 2016		Sheet 30 of 53

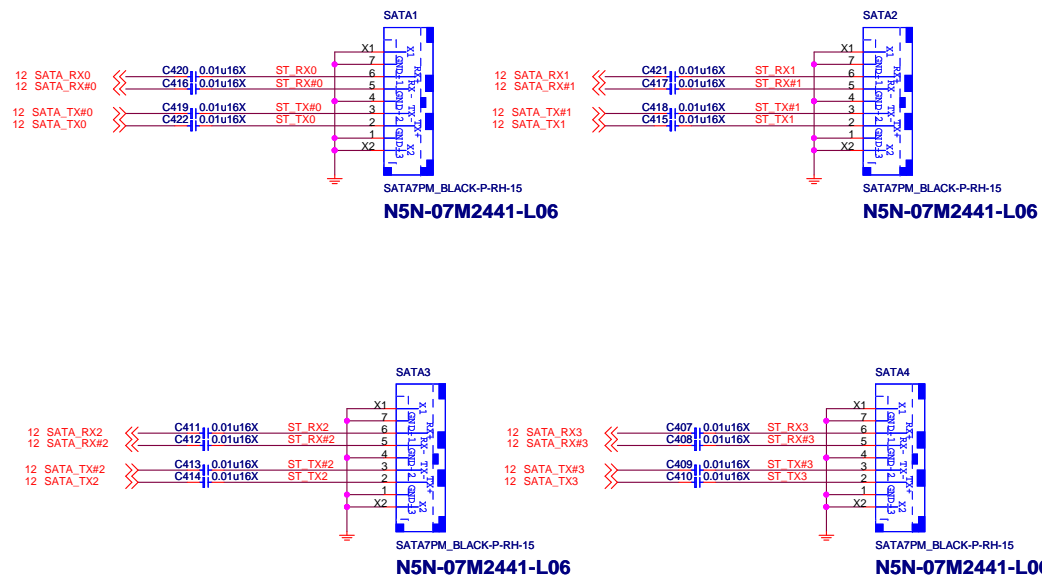
USB2.0 HUB

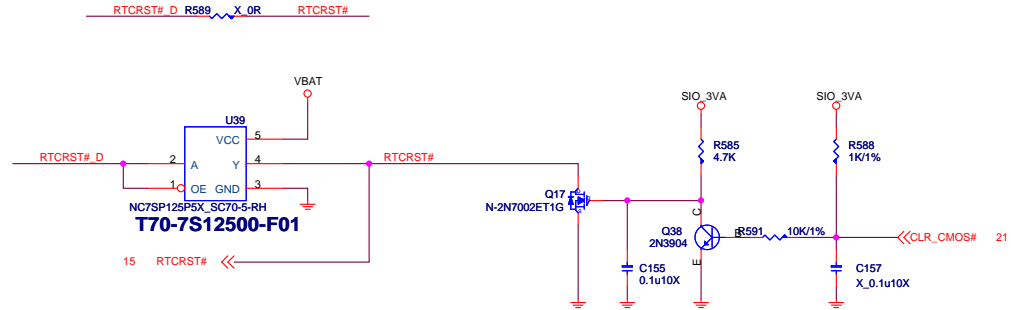
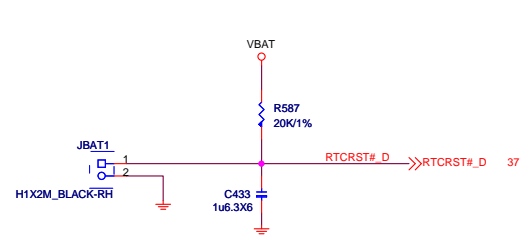
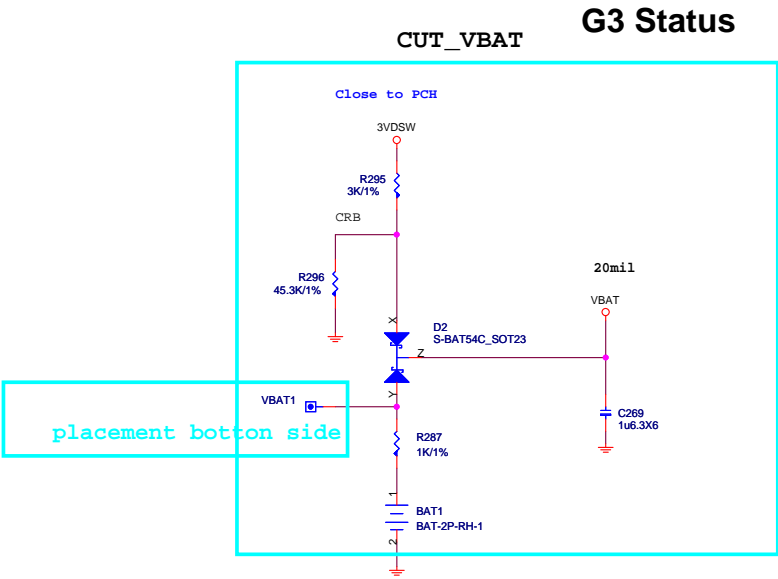
4-port at high-speed mode. --> 58.6mA



[illegible]







tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

	R589	U39	R587	C433
USE U39				
Auto CLR_CMOS	X	O	O	O
NOT USE U39				
Auto CLR_CMOS	O	X	X	X

15 PCH_SPI0_MOSI << PCH_SPI0_MOSI
15 PCH_SPI0_MISO << PCH_SPI0_MISO
15 PCH_SPI0_CLK << PCH_SPI0_CLK
15 PCH_SPI0_CS0# << PCH_SPI0_CS0#
15 PCH_SPI0_IO2 << PCH_SPI0_IO2
15 PCH_SPI0_IO3 << PCH_SPI0_IO3

- 1.DPWROK比RSMRST#早起，拉PWROK是避免ME code會跑
- 2.開機狀態下VCC3起來，SIO丟出PWROK，不看RSMRST#
- 3.第一次上電SLP_S3# 拉HI，用RSMRST#卡不住

15,21 PCH_DPWROK >> D21 X S-RB751V-40_SOD323-RH
15,21 RSMRST# >> D18 S-RB751V-40_SOD323-RH
15,21 CHIP_PWGD >> D17 S-RB751V-40_SOD323-RH

D01-RB751V0-W12
D01-RB751V0-W12
D01-RB751V0-W12

21,37 SYS3VSB_OFF >> D16 S-RB751V-40_SOD323-RH

D01-RB751V0-W12

Flash ROM的 3VSB power要KEEP住

SPI CS# < 25pF
D0G-0402510-S10

2014.08.25

Close to JSP11

2014.12.15

PCH_SPI0_MISO R551 X 1K
PCH_SPI0_MOSI R583 X 1K

2015.01.15

2014.09.24 For intel MOW36 update
pull down resistor on SPI0_IO3 is needed for SKL S/H
platforms with pre-ES1/ES1 samples.
20150115
update this issue for PRE-ES2/ES2 refer mail 20150115
From syng

* if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002
* if you support Standby power in S5 Status(Ex: PCH is B75 Chipset), component Q14.G Pull-high to ATX_5VSB, Q14 must select "Vth" under 1V (Component Suggestion as below)

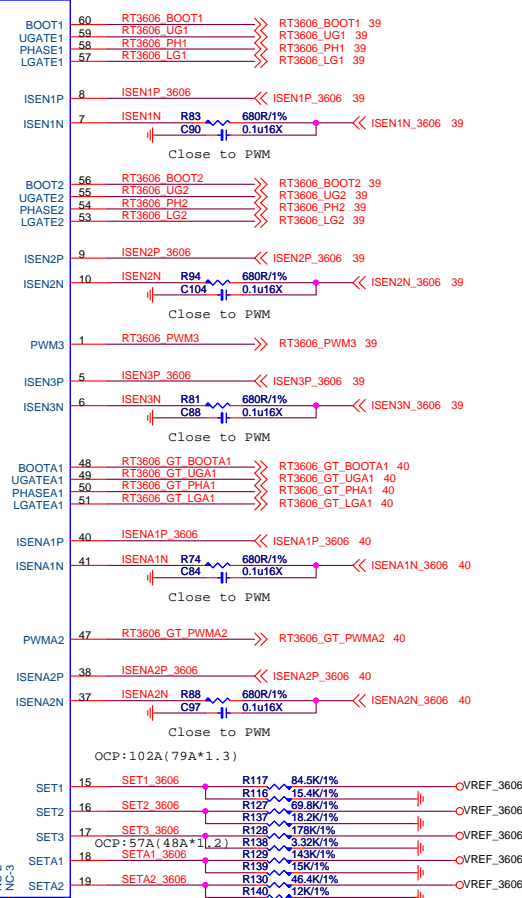
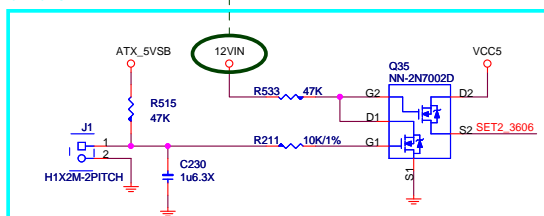
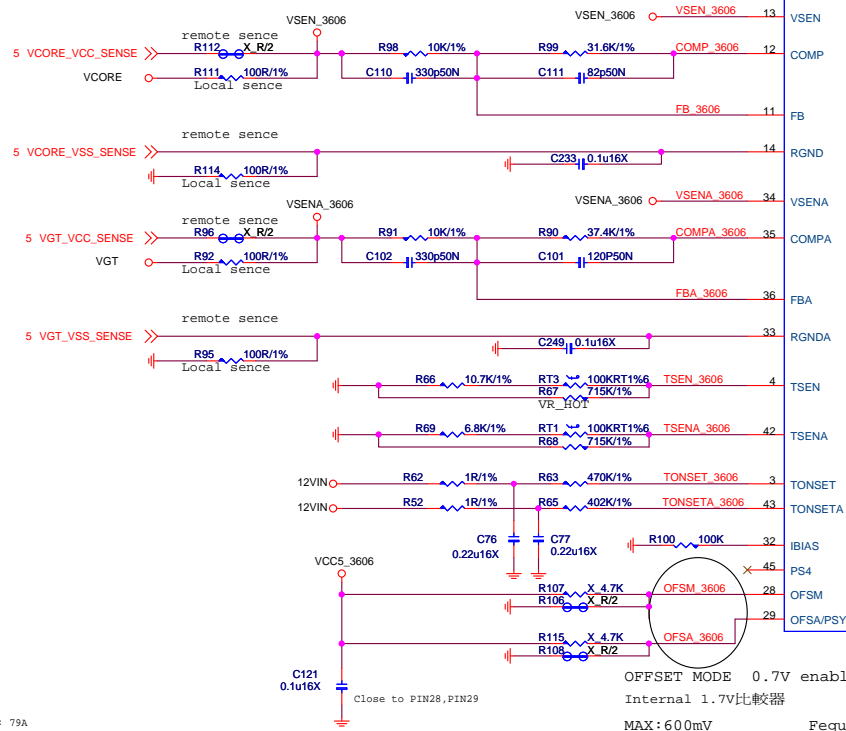
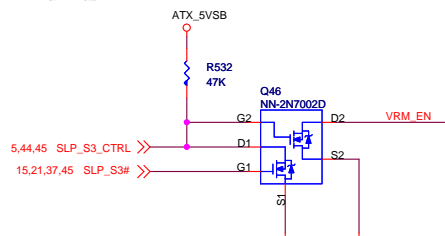
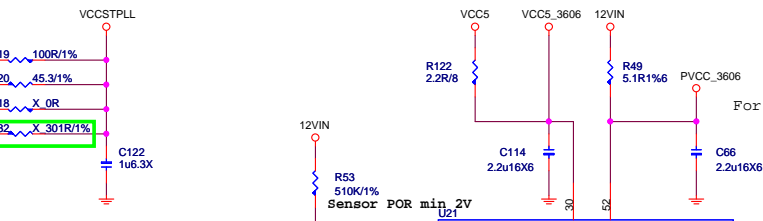
D03-0341409-A68 / D03-0230019-A30



MICRO-STAR INT'L CO.,LTD

MS-7A49

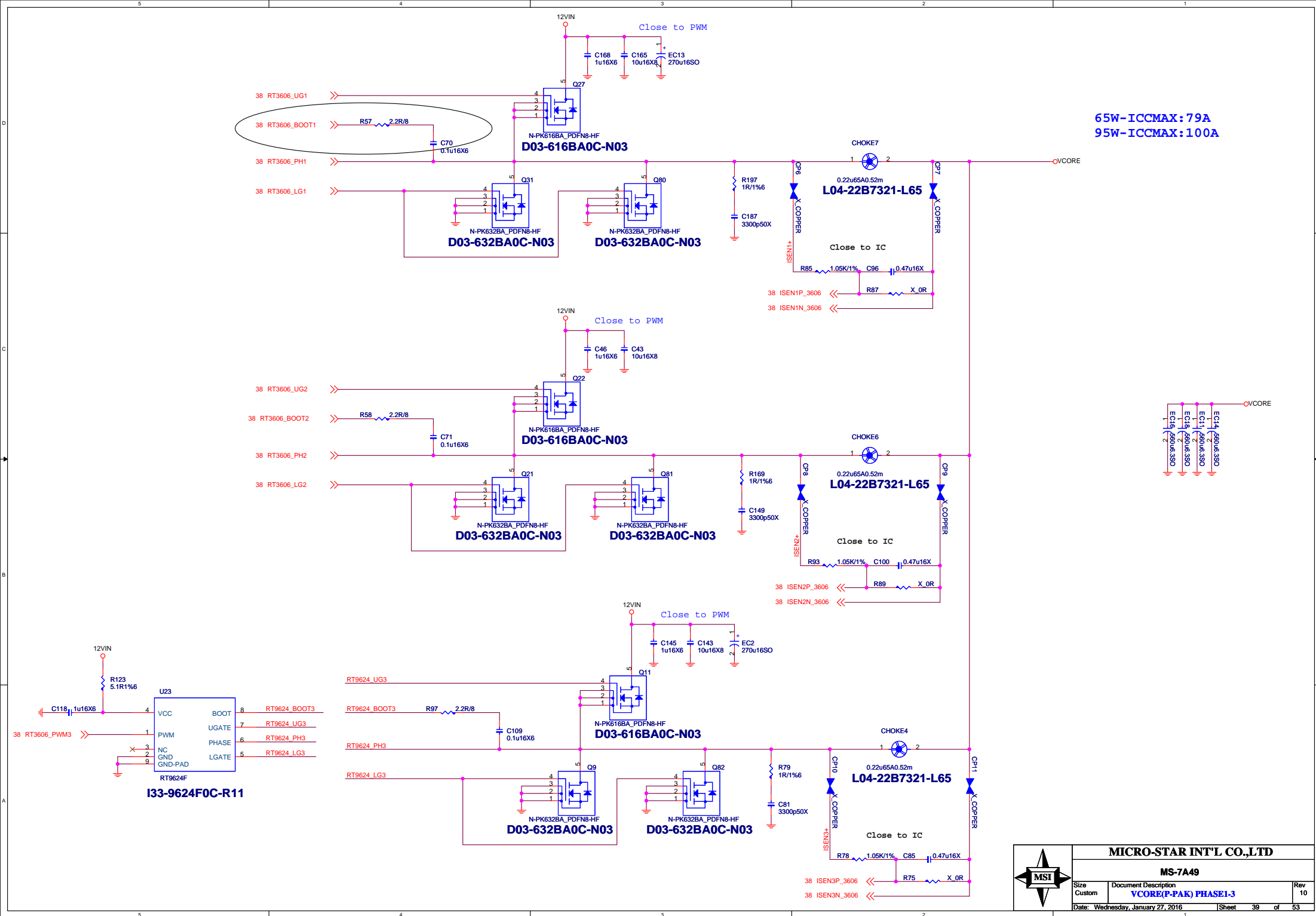
Size Custom	Document Description BIOS ROM	Rev 10
Date: Wednesday, January 27, 2016	Sheet 36 of 53	

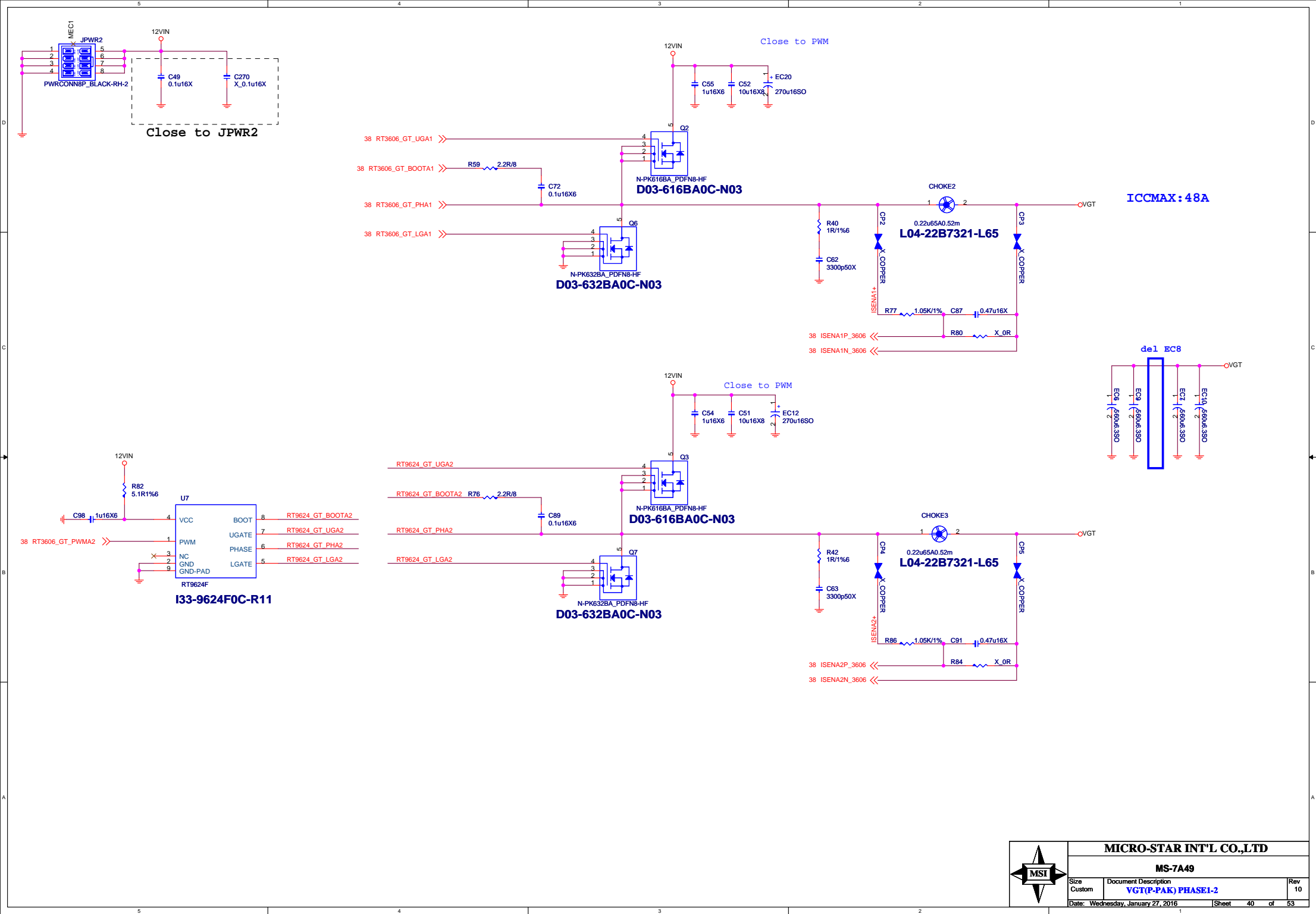


```
SET1 control ICCMAX,OCP setting
SET2 control Internal compensation
SET3 control VR address
SETA1 control ICCMAX,OCP setting
SETA2 control Internal compensation
```



MICRO-STAR INT'L CO.,LTD			
MS-7A49			
Size Custom	Document Description PWM-RT3606BC		Rev 10
Date: Wednesday, January 27, 2016		Sheet 38 of 53	





MICRO-STAR INT'L CO.,LTD			
MS-7A49			
Size	Document Description	Rev	
Custom	VGT(P-PAK) PHASE1-2	10	
Date: Wednesday, January 27, 2016		Sheet	40 of 53

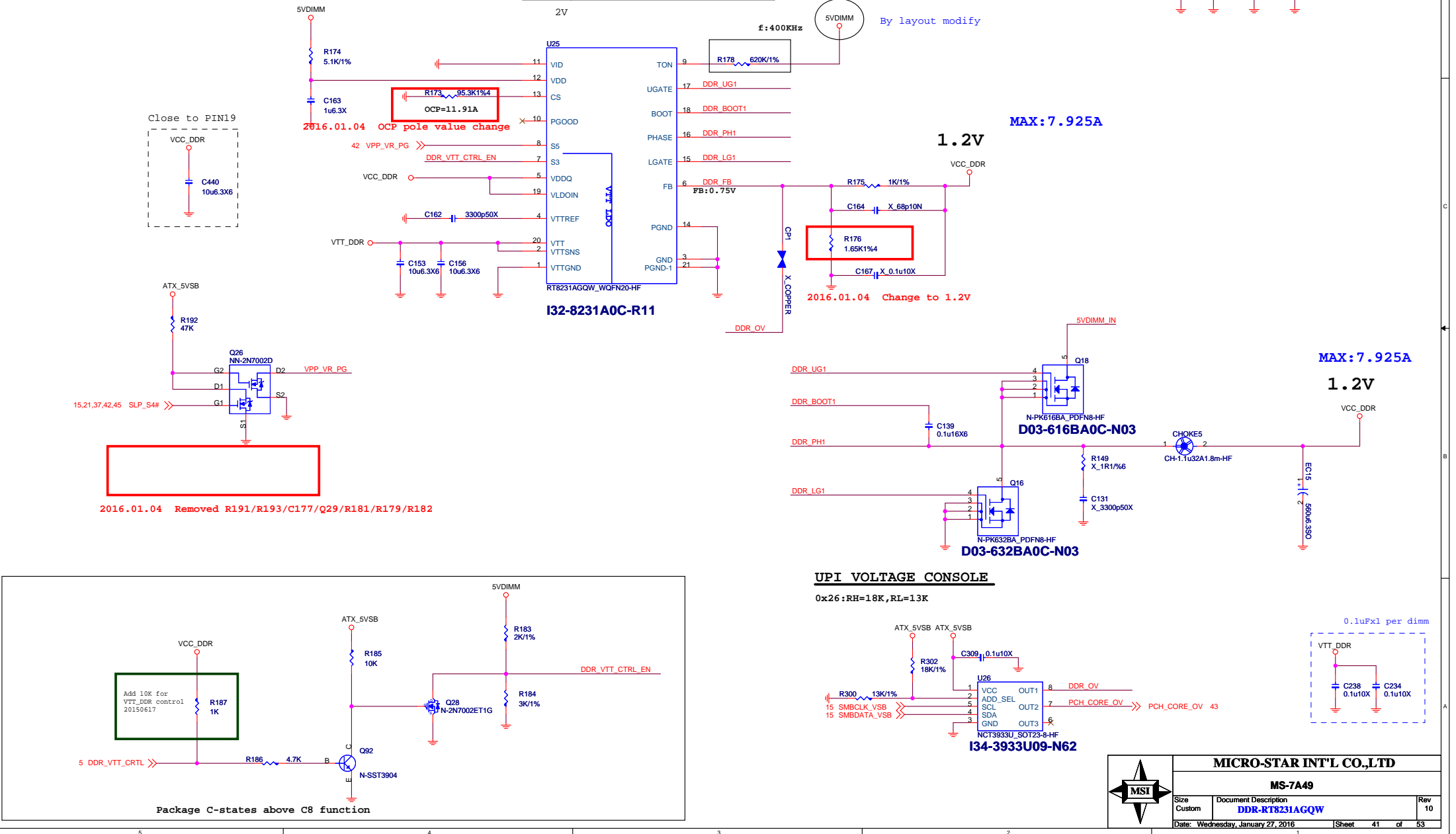
DDR4_1.2V 2.8A+ 4.75A+0.375A=7.925

2.8A FOR CPU
4.75A FOR 2DIMM DDR4
0.375A FOR VTT_DDR

OCP = 7.925A*1.5=11.8875A
Current limit= 95.3K(R173)*5uA/10/4mohm)=11.91A

VID	Reference Voltage (V)
H	0.675
L	0.75

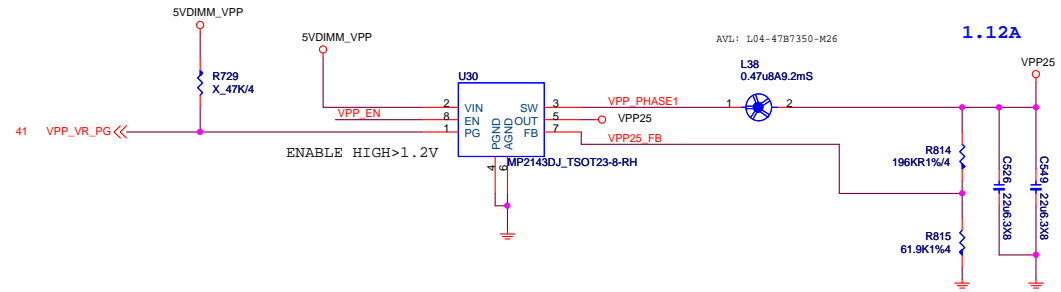
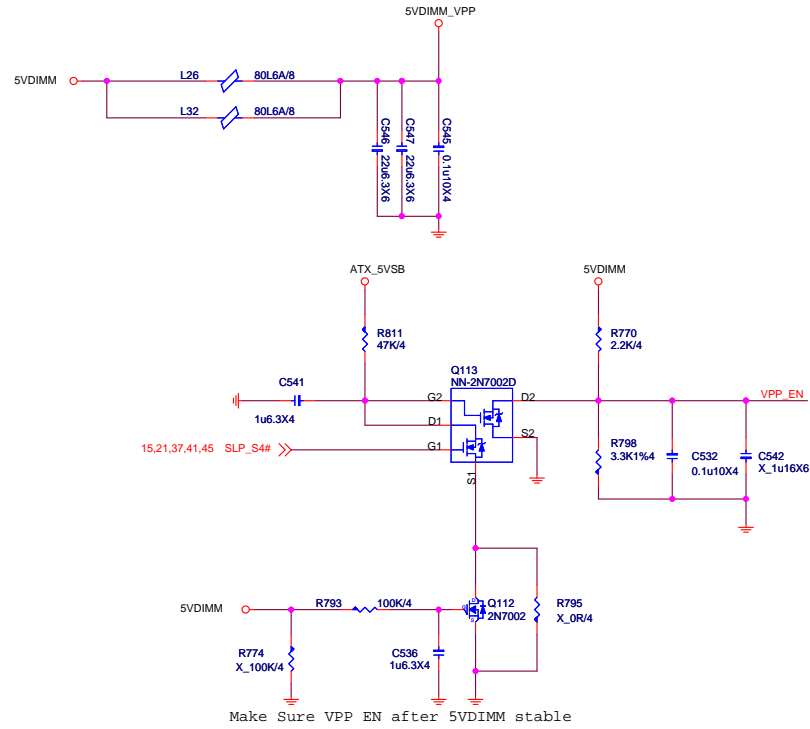
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 7.925 * 0.42
= 3.384A



2016.01.04 Add VPP25 POWER IC

2DIMM :1.12A FOR DDR VPP2.5V

VPP25 Power 2.5V; 1.12A



PCH 1VSB

PCH_1VSB = 8.68A

VCCIO = 5.5A

VCCSTPLL_EN = 0.25A

USB 3.0 Port: 132mA*4=528mA

Each PCIe Gen3 Lane: 154mA*3=462mA

DMI x4: 700mA

First SATA Gen3 Port: 54mA

Each Additional SATA Gen3 Port: 132mA*3=396mA

(6.54A + 0.132*4 + 0.154*3 + 0.7 + 0.054 + 0.132*3) = 8.68A

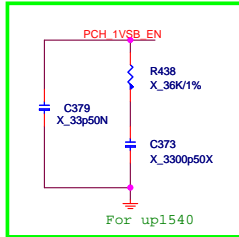
2015.04.23 change to UP1540
2015.08.07 change to RT8125E

OCP = 21.65A

Rocset = 1.5 * I_{max} * R_{ds(on)}(low) / Iocset
= 1.5 * 14.43 * 4mohm / 10uA
= 9.76K

Roccs: 9.76K, OCP:
D03-4C05N03-005 : 21A
D03-632BA0C-N03 : 26.25A
use UBIQ MOS need Check

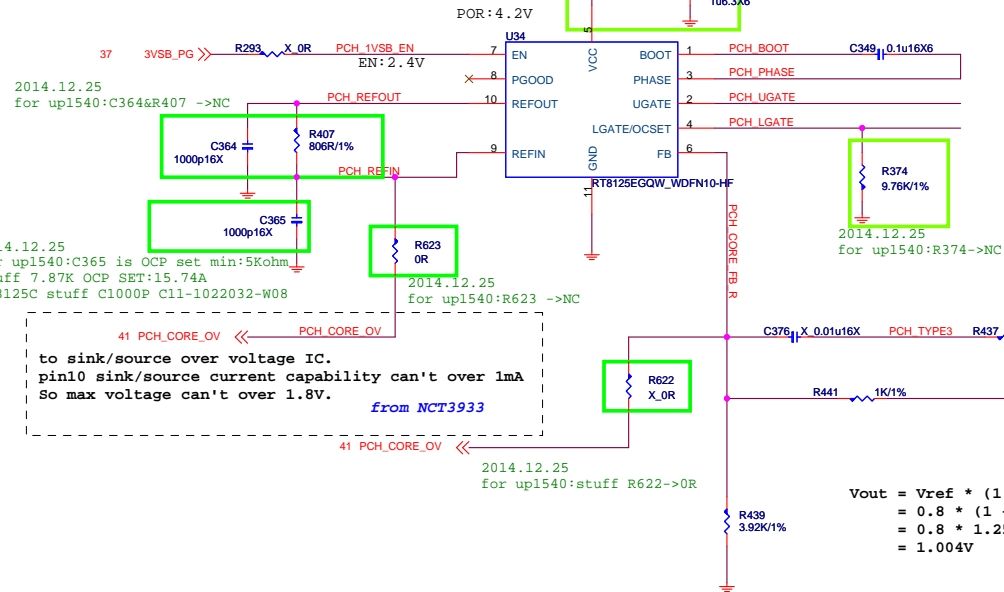
2014.08.22 close to U34



2015.01.22
for up1540:stuff R438->36K,
C379->NC, C373->3.3nF
for RT8125:R438.C379.C373->NC

R_{ds(on)}(low) 4.5V
D03-4C05N03-005 : 5 mohm
D03-632BA0C-N03 : 4mohm
D03-3056M00-U47 : 6.2mohm

2015.01.22
for up1540:R96->2.2R, C84->1uF
for RT8125:R96->10R, C84->1uF



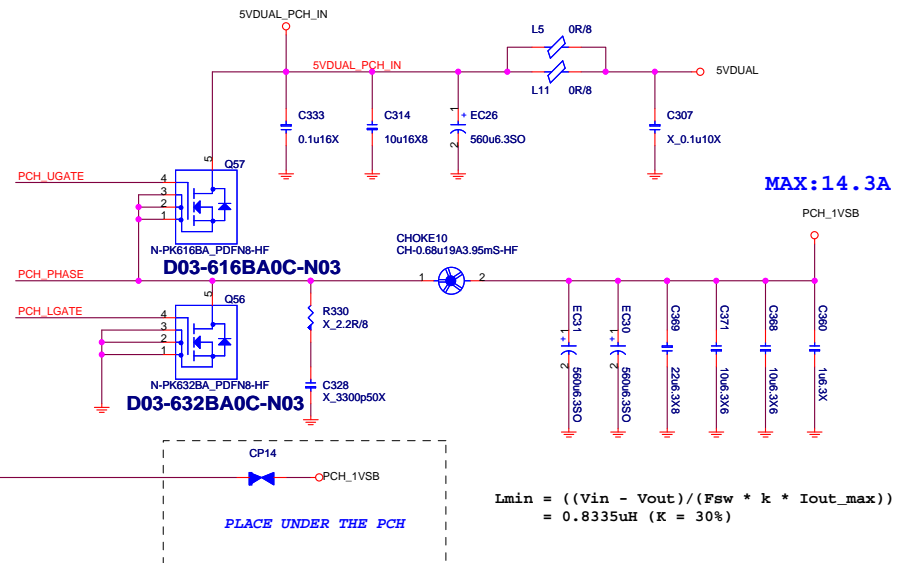
2014.12.25
for up1540:C364&R407 ->NC
2014.12.25
for up1540:C365 is OCP set min:5Kohm
stuff 7.87K OCP SET:15.74A
RT8125C stuff C1000P C11-1022032-W08

41 PCH_CORE_OV << PCH_CORE_OV
to sink/source over voltage IC.
pin10 sink/source current capability can't over 1mA
So max voltage can't over 1.8V.
from NCT3933

2014.12.25
for up1540:stuff R622->0R

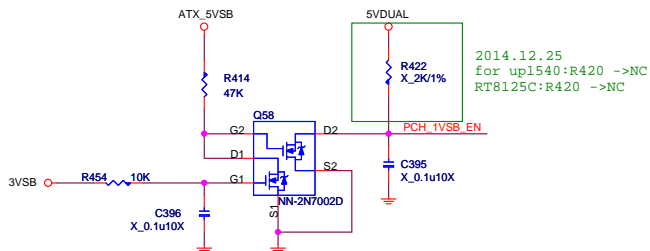
V_{out} = V_{ref} * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

I_{rms} = I_{out} * SQRT((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))
= 14.3 * 0.4
= 5.72 A



MAX: 14.3A

I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})
= 0.8335uH (K = 30%)



2014.12.25
for up1540:R420 ->NC
RT8125C:R420 ->NC

MICRO-STAR INT'L CO.,LTD			
MS-7A49			
Size	Document Description	Rev	
Custom	PCH Core power	10	
Date:	Wednesday, January 27, 2016	Sheet	43 of 53

SA Power:1.05V,11.1A

$$OCP = 11.1A * 1.4 = 15.54A$$
$$R_{ocs}(R15) = OCP * R_{dson}(\text{Low side}) 3.3\text{mohm} / 10\mu A$$
$$= 15.54 * (3.3) \text{ mohm} / 10 \mu\text{A}$$
$$= 5.2836 \text{ Kohm}$$

Rocs:5.2836K,OCP:

D03-4C05N03-005 : 20.99A

D03-632BA0C-N03 : 15.54A

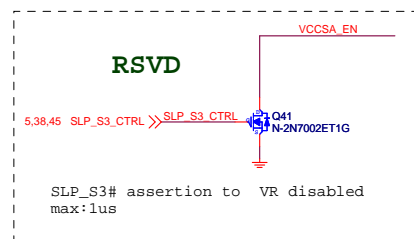
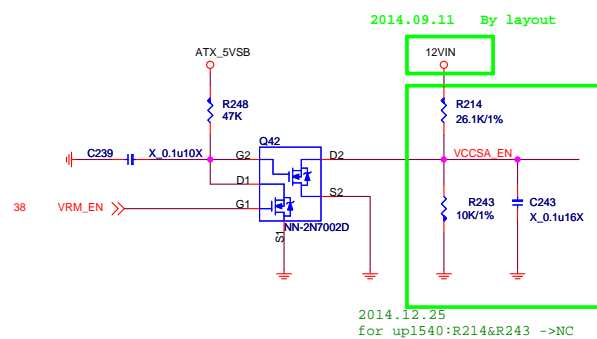
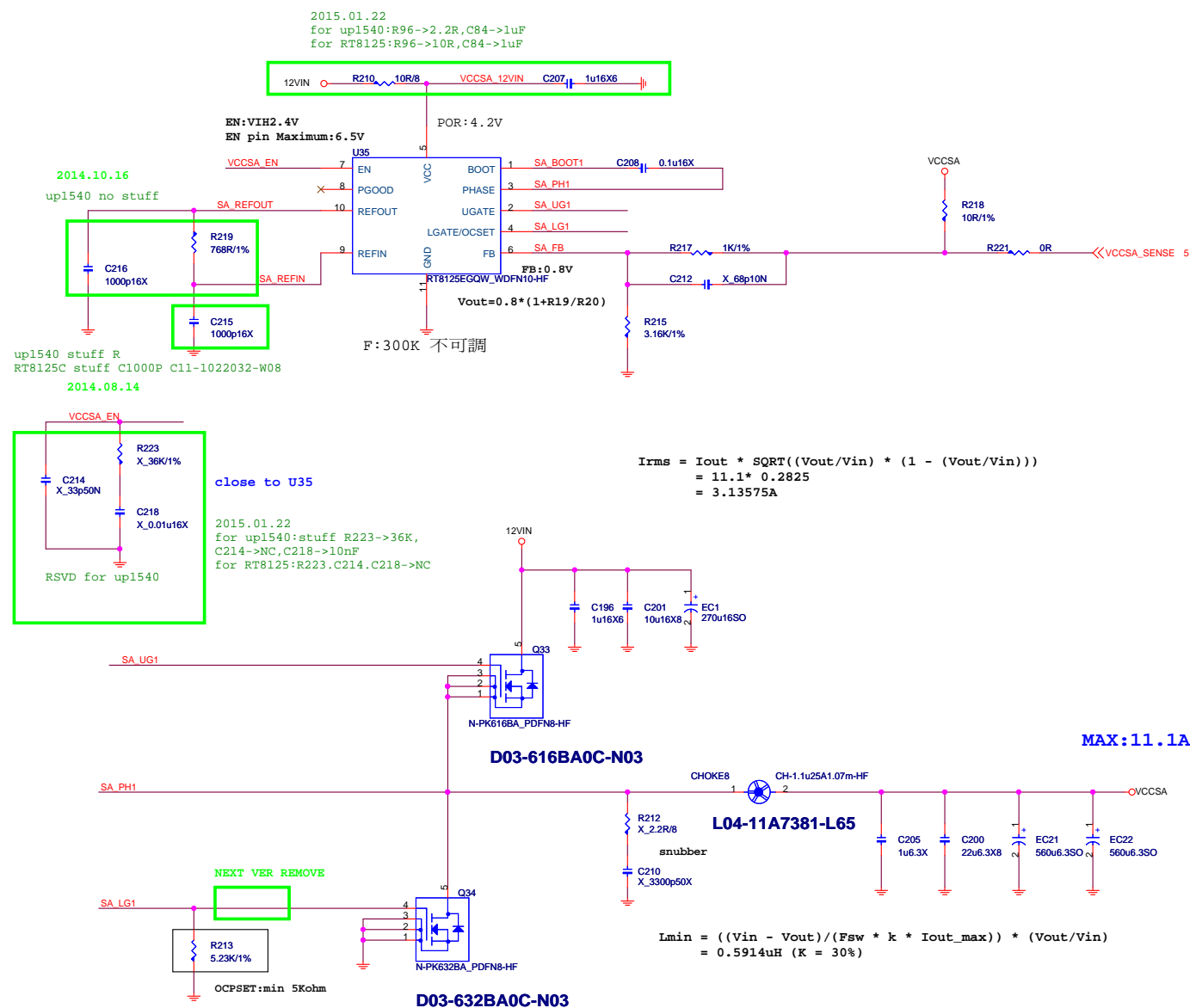
use UBIQ MOS need Check

$R_{\text{dson}}(10V)$

D03-4C05N03-005 : 3.4mohm

D03-632BA0C-N03 : 3.3mohm

D03-3056M00-U47 : 4.2mohm



MICRO-STAR INT'L CO.,LTD

MS-7A49

Size	Document Description	Rev
------	----------------------	-----

Custom	VCCSA - POWER RT8125C	10
--------	-----------------------	----

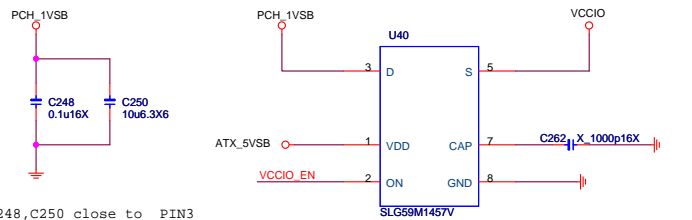
Date: Wednesday, January 27, 2016	Sheet 44 of 53
-----------------------------------	----------------

2015.10.26 change to SLG59M1457 load switch, Pwr source by PCH_1VSB

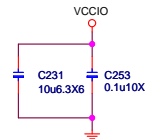
VCCIO

0.95V; 5.5A

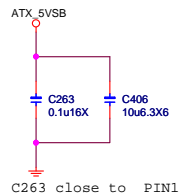
Source 1.00V



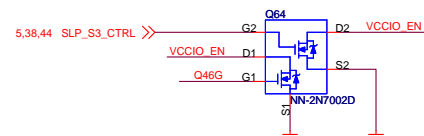
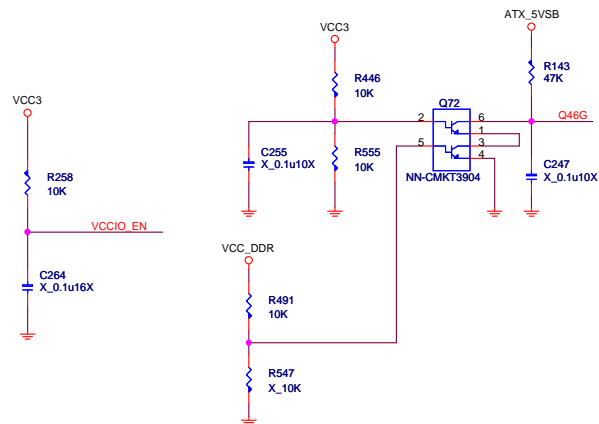
MAX: 5.5A



VCCIO ramped and stable before
beginning of VCCOPC/VCCEPIO ramp



VCCIO_EN

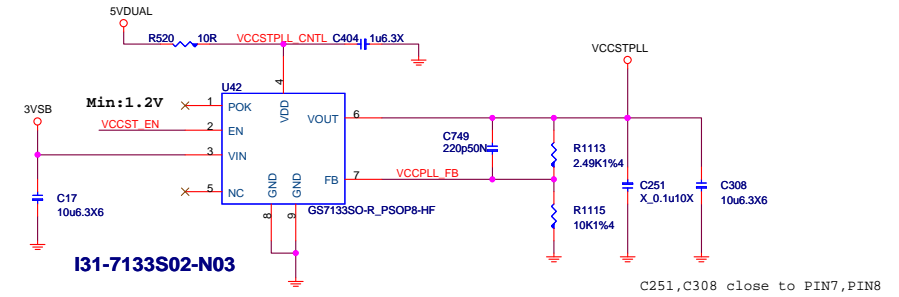


2015.10.26 change to GS7116

VCCSTPLL

1.00V; 250mA

MAX: 250mA

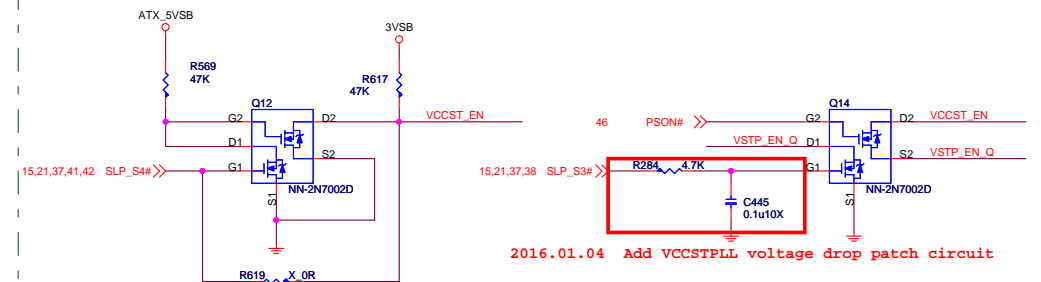


I31-7133S02-N03

VCCST/PLL stable 1ms before PROCPWRGD

VCCSTPLL_EN

20151623 Fix G3->S5 PWR auto enable



2016.01.04 Add VCCSTPLL voltage drop patch circuit

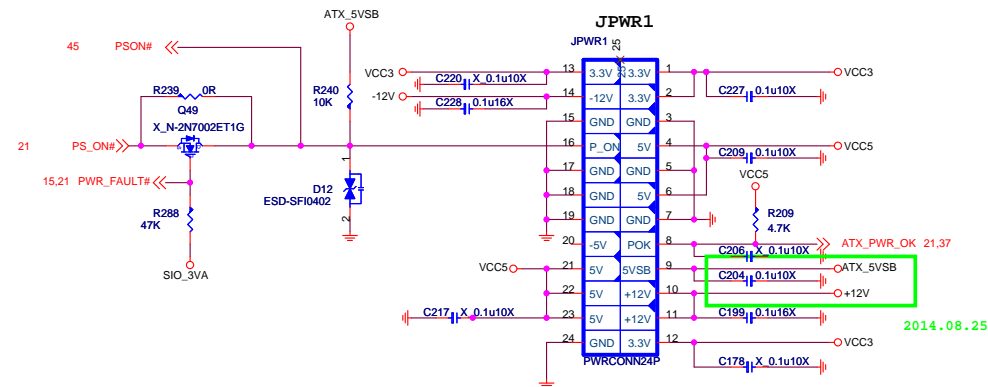


MICRO-STAR INT'L CO.,LTD

MS-7A49

Size	Document Description	Rev
Custom	VCCIO - POWER NB671	10
Date:	Wednesday, January 27, 2016	Sheet 45 of 53

ATX POWER CONNECTOR



2016.01.13 Removed

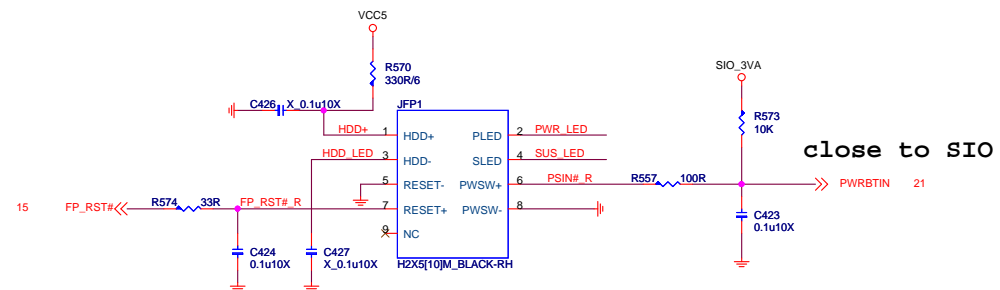
PWR_FAULT# LED

上1K是解決航嘉200W(huntkey)power supply的問題,加1K是為了不讓ATX_5Vsb空載而產生震盪

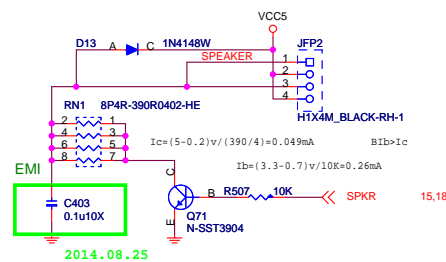
2016.01.13 Removed

MSI LED

FRONT PANNEL

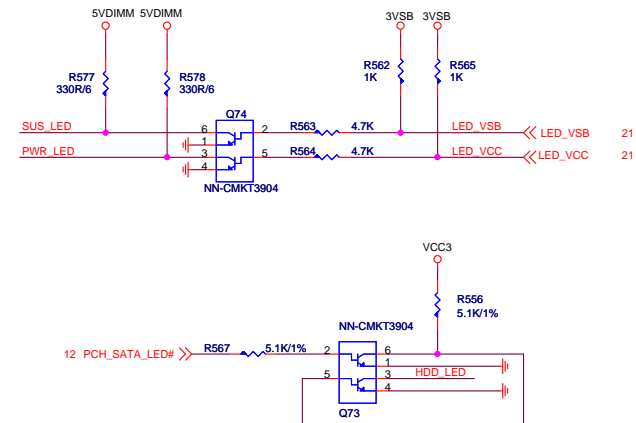


Speaker Pin Header

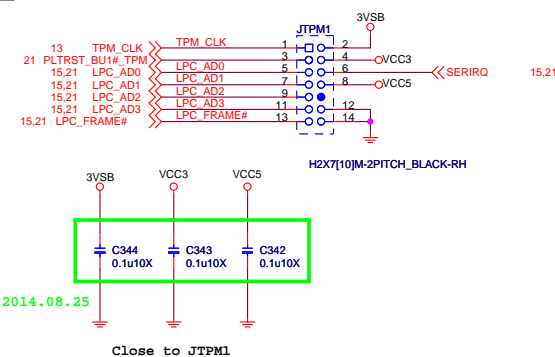


R=390 Ohm
 $I=(5-0.2)/R=0.0123\text{ A}$
 $W=0.0123\text{ A} \times 5\text{ V}=0.0615\text{ W}$ (夠耐電阻)
 $R=1/16\text{ W}=0.062\text{ W}$

LED (for NV6793D)



TPM

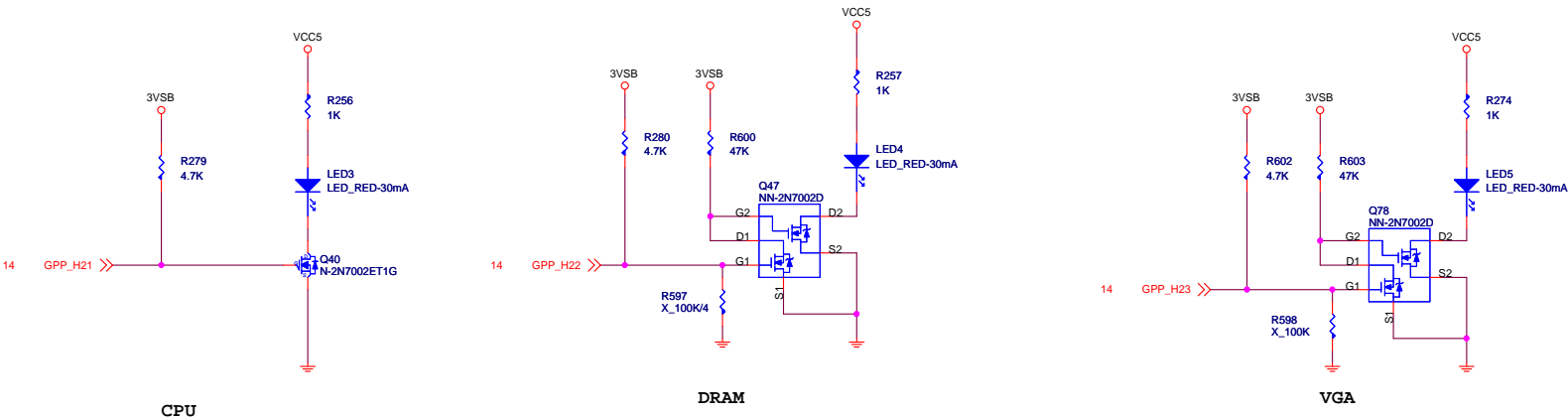


MICRO-STAR INT'L CO.,LTD

MS-7A49

Size	Document Description	Rev
Custom	ATX F_Panel/TPM/MSI_LED	10
Date:	Wednesday, January 27, 2016	Sheet 46 of 53

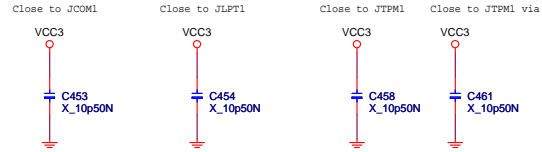
DEBUG LED

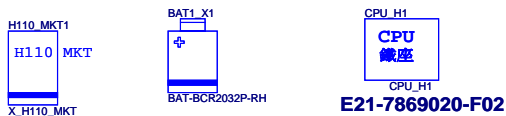
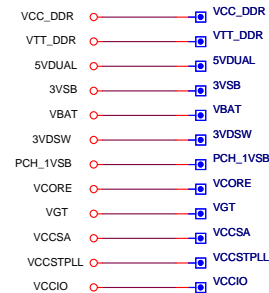
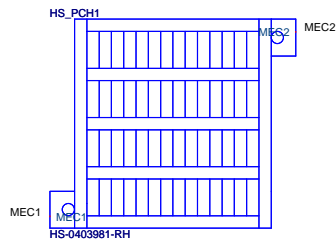


<div><div>GPIO</div><div>LED</div></div>	GPP_H21	GPP_H22	GPP_H23
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

- 關機斷電狀態下，3個LED先維持default全暗，開機通電後：
- 1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
 - 2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
 - 3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
 - 4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

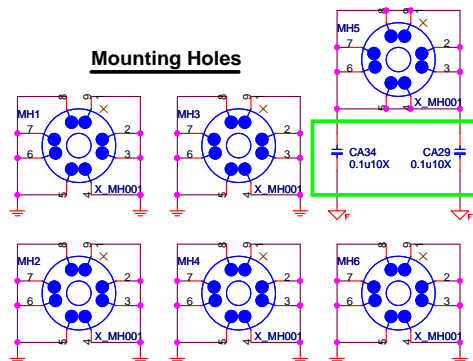
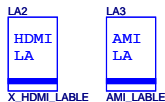
EMI CAP



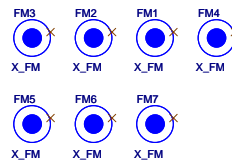


PK0-0799311-G37

PK0-0799311-G37, 精成-深圳, 20, 寶安恩斯邁廠 (MSIS) 4, Coffee
PK0-0799311-E48, 競華, 15, 寶安恩斯邁廠 (MSIS) 4, Coffee



Optical Fiducial Marks-120



Simulation



OPT	Configure	BOM	Function
		601-7993-01S	MS-7993 10 B150M PRO-VDL D3, B150,LGA1151, 2DDR3,1PCIEx16,1PCIEx1,2PCI,4SATA3, 4USB3.1(Gen1),6USB2.0,HD Audio,Gb LAN,DVI-D,VGA,COM
A		601-7993-02S	MS-7993 10 OPT:A H110M PRO-VDL D3, H110,LGA1151, 2DDR3,1PCIEx16,1PCIEx1,2PCI, 4SATA3, 4USB3.1(Gen1),6USB2.0,HD Audio,Gb LAN,DVI-D,VGA,COM
A		601-7993-03S	MS-7993 11 OPT:A H110M PRO-VDL D3, H110,LGA1151, 2DDR3,1PCIEx16,1PCIEx1,2PCI, 4SATA3, 4USB3.1(Gen1),6USB2.0,HD Audio,Gb LAN,DVI-D,VGA,COM
A		601-7993-010	MS-7993 11 OPT:A H110M PRO-VDL D3, H110,LGA1151, 2DDR3,1PCIEx16,1PCIEx1,2PCI, 4SATA3, 4USB3.1(Gen1),6USB2.0,HD Audio,Gb LAN,DVI-D,VGA,COM
B		601-7993-020	MS-7993 11 OPT:B H110M_S02 PRO-VDL D3, H110,LGA1151, 2DDR3,1PCIEx16,1PCIEx1,2PCI, 4SATA3, 4USB3.1(Gen1),6USB2.0,HD Audio,Gb LAN,DVI-D,VGA,COM

MICRO-STAR INT'L CO.,LTD

MS-7A49

Size Custom	Document Description Manual Parts	Rev 10
Date: Wednesday, January 27, 2016		Sheet 49 of 53